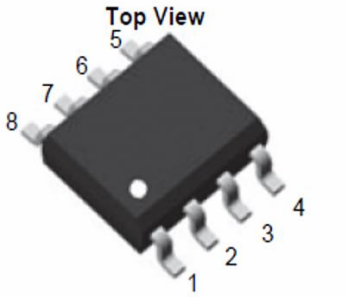
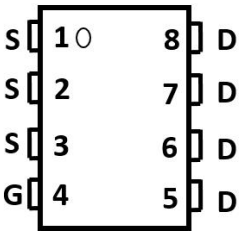
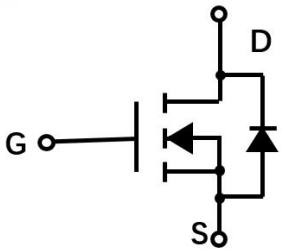
RoHS COMPLIANT

N-Channel Enhancement Mode Field Effect Transistor





SOP-8



Product Summary

- V_{DS} 100V
- I_D 12A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜17 mohm
- 100% UIS Tested
- 100% ▽V_{DS} Tested

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- Motor control and drive
- Battery management
- UPS

■ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter		Symbol	Maximum	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	12	A
	T_A =100℃		7.6	
Pulsed Drain Current [A]		I_{DM}	120	A
Avalanche Energy, Single Pulse(L=10mH)		E_{AS}	500	mJ
Total Power Dissipation		P_D	3.3	W
Thermal Resistance Junction-Lead		$R_{\theta JL}$	19	℃/ W
Thermal Resistance Junction-to-Ambient [B]	t≤ 10s	$R_{\theta JA}$	38	
	Steady State		66	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJS12N10A	F2	Q12N10	4000	8000	64000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V, T_J=25℃			1	μA
		V_{DS}=80V,V_{GS}=0V, T_J=85℃			50	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	2.0	3.0	4.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=12A		14	17	mΩ
Transconductance	g_{fs}	V_{DS} =10V, I_D =10A		26		S
Diode Forward Voltage	V_{SD}	I_S=12A,V_{GS}=0V		0.9	1.2	V
Maximum Body-Diode Continuous Current	I_S				12	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHZ		3870		pF
Output Capacitance	C_{oss}			185		
Reverse Transfer Capacitance	C_{rss}			157		
Switching Parameters						
Total Gate Charge (10V)	Q_g	V_{GS}=10V,V_{DD}=50V,I_D=12A		80		nC
Gate Source Charge	Q_{gs}			12		
Gate Drain Charge	Q_{gd}			25		
Turn-on Delay Time	$t_{d(on)}$	V_{GS}=10V,V_{DD}=50V, I_D=12A, R_{GEN}=1Ω		13		ns
Turn-on Rise Time	t_r			14		
Turn-off Delay Time	$t_{d(off)}$			25		
Turn-off Fall Time	t_f			10		
Reverse Recovery Time	t_{rr}	V_R =50V, I_F =12A, dI_F/dt=100A/μs		33		ns
Reverse Recovery Charge	Q_{rr}			54		nC

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. Surface Mounted on FR4 Board, t ≤ 10 sec.

■ Typical Performance Characteristics

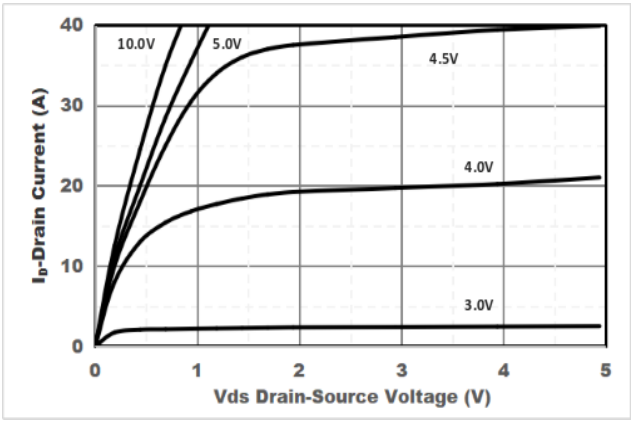


Figure1. Output Characteristics

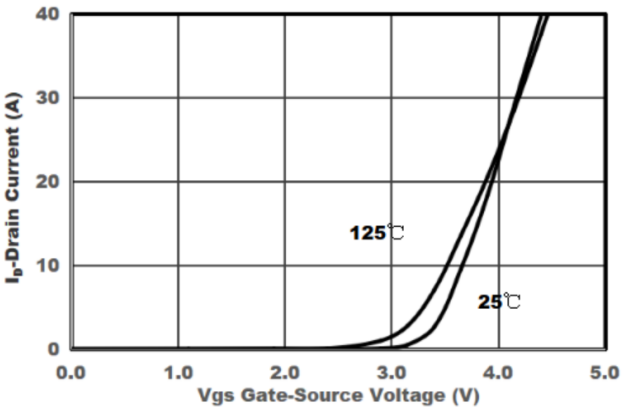


Figure2. Transfer Characteristics

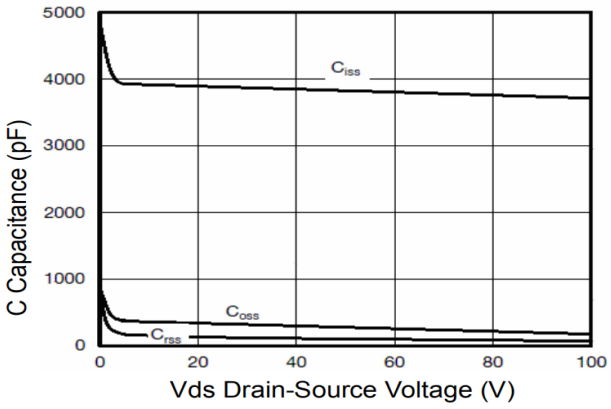


Figure3. Capacitance Characteristics

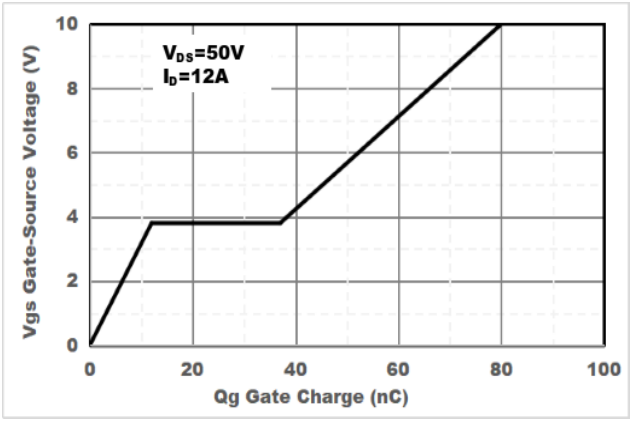


Figure4. Gate Charge

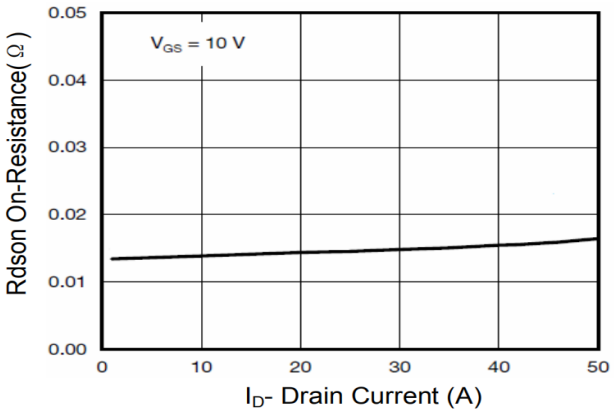


Figure5. Drain-Source on Resistance

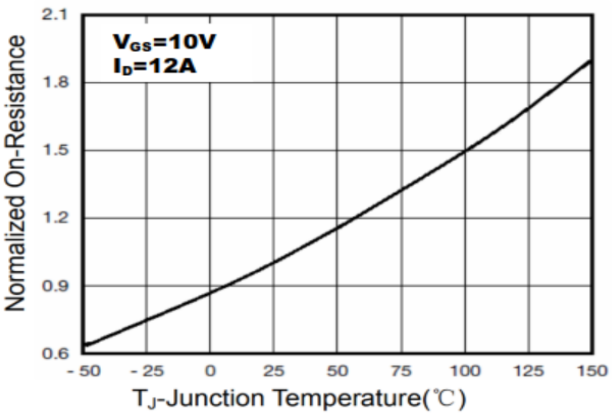


Figure6. R_{dson} - Junction Temperature

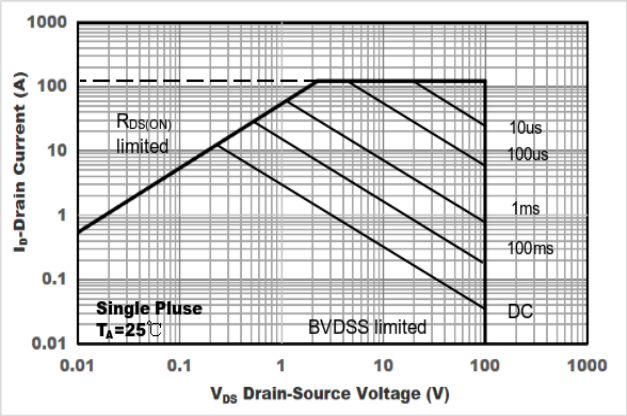


Figure7 Safe Operation Area

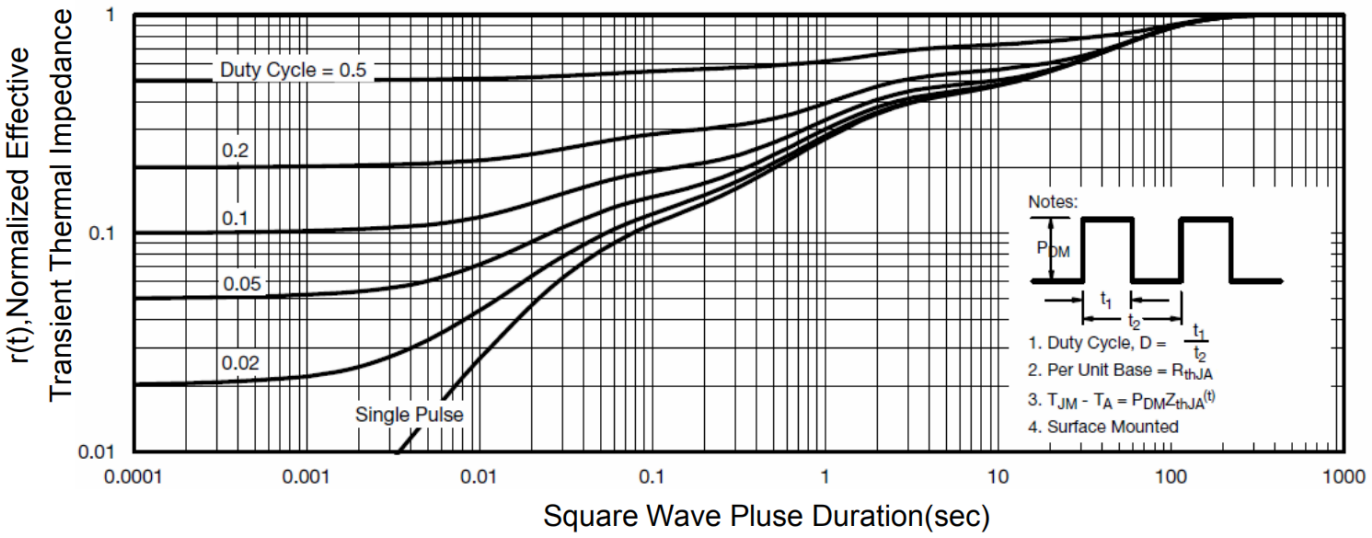


Figure 8. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

Figure A: Gate Charge Test Circuit & Waveforms

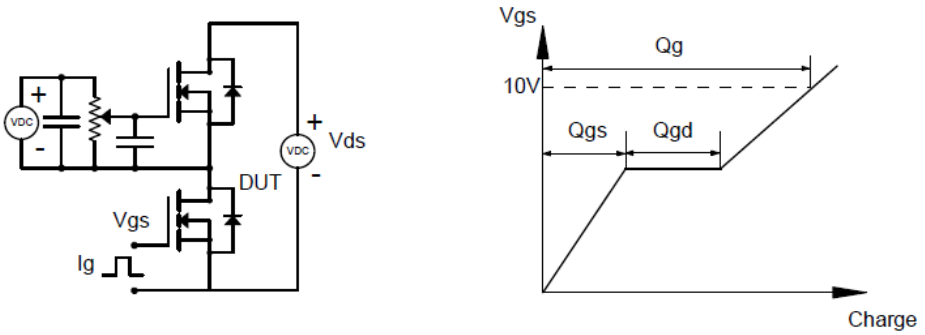


Figure B: Resistive Switching Test Circuit & Waveforms

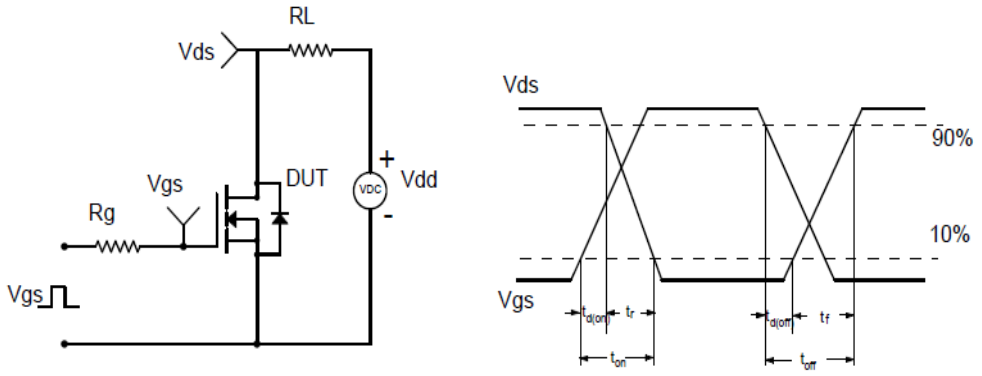


Figure C: Unclamped Inductive Switching (UIS) Test

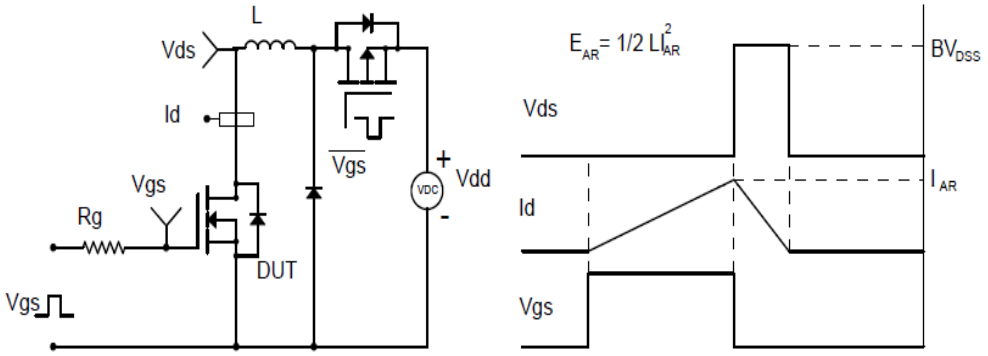
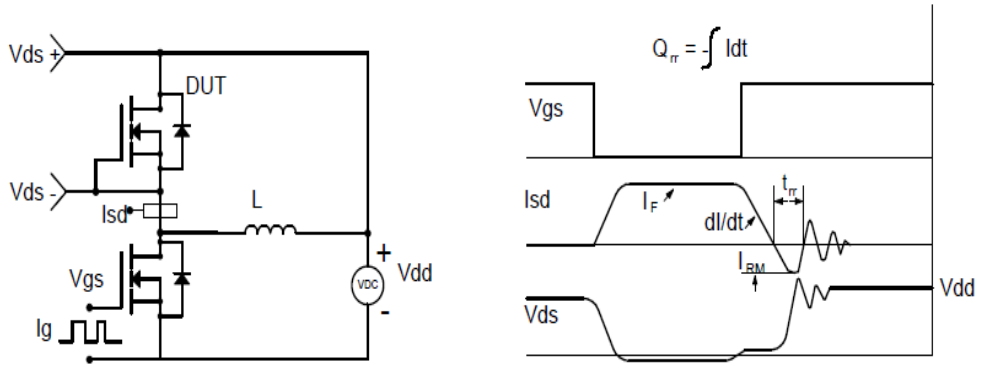
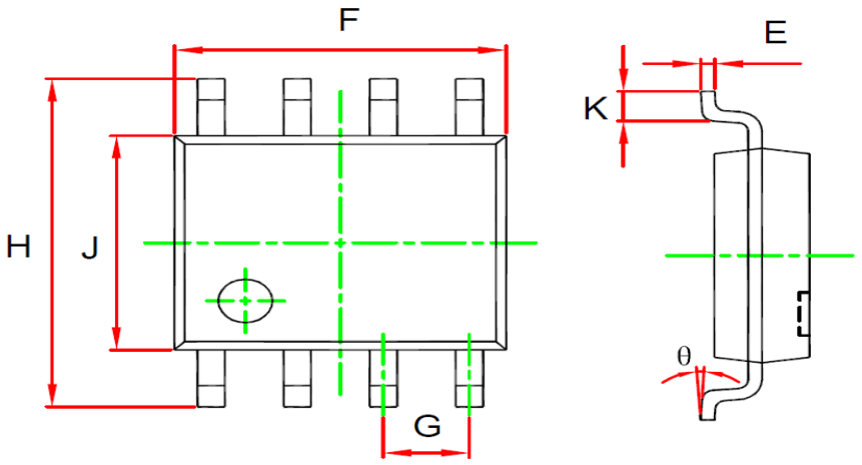
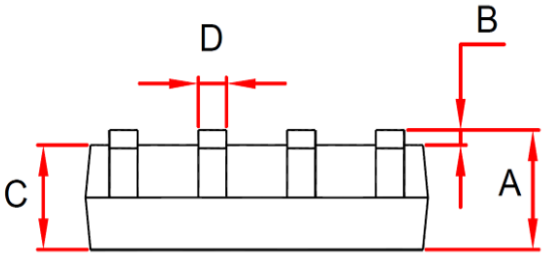


Figure D: Diode Recovery Test Circuit & Waveforms



■ SOP-8 Package information





DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.350	1.750	
B	0.004	0.010	0.100	0.250	
C	0.053	0.061	1.350	1.550	
D	0.013	0.020	0.330	0.510	
E	0.007	0.010	0.170	0.250	
F	0.189	0.197	4.800	5.000	
G	0.050 (BSC)		1.270 (BSC)		
H	0.228	0.244	5.800	6.200	
J	0.150	0.157	3.800	4.000	
K	0.016	0.050	0.400	1.270	
θ	0°	8°	0°	8°	

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