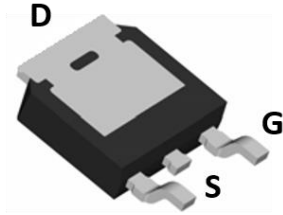
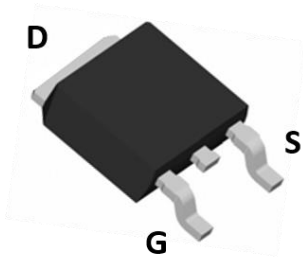
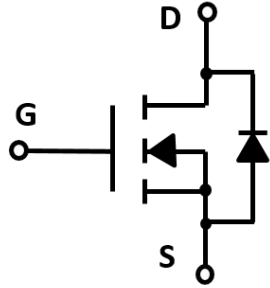


N-Channel Enhancement Mode Field Effect Transistor



TO-252



Product Summary

- V_{DS} 40V
- I_D 70A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <8.0 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <10 mohm
- 100% UIS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	70	A
	$T_C=100^\circ\text{C}$		49	
Pulsed Drain Current ^A		I_{DM}	270	A
Total Power Dissipation	$T_C=25^\circ\text{C}$	P_D	64	W
	$T_C=100^\circ\text{C}$		32	W
Single Pulse Avalanche Energy ^B		E_{AS}	110	mJ
Thermal Resistance Junction-to-Case ^C		$R_{\theta JC}$	2.3	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	$-55 \sim +175$	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD70N04A	F2	YJD70N04A	2500	2500	25000	13" reel



YJD70N04A

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA		40			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V	T _J =25℃			1	μA
			T _J =55℃			5	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V				±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA		0.7	1.2	2.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =20A			6.5	8.0	mΩ
		V _{GS} = 4.5V, I _D =10A			7.7	10	
Diode Forward Voltage	V _{SD}	I _S =20A, V _{GS} =0V			0.8	1.2	V
Maximum Body-Diode Continuous Current	I _S					70	A
Dynamic Parameters							
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, f=1MHZ			1200		pF
Output Capacitance	C _{oss}				240		
Reverse Transfer Capacitance	C _{rss}				128		
Switching Parameters							
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =20V, I _D =20A			24		nC
Gate-Source Charge	Q _{gs}				4.9		
Gate-Drain Charge	Q _{gd}				5		
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us			21		ns
Reverse Recovery Time	t _{rr}				40		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =20V, I _D =2A, R _L =1Ω R _{GEN} =3Ω			6		
Turn-on Rise Time	t _r				36		
Turn-off Delay Time	t _{D(off)}				29		
Turn-off fall Time	t _f				7		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. T_J=25℃, V_{DD}=35V, V_G=20V, L=0.5mH.

C. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

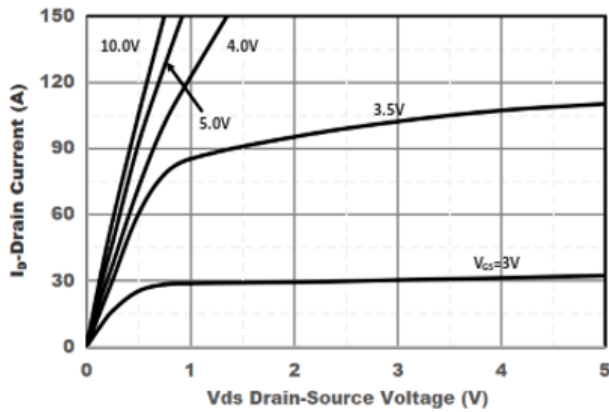


Figure1. Output Characteristics

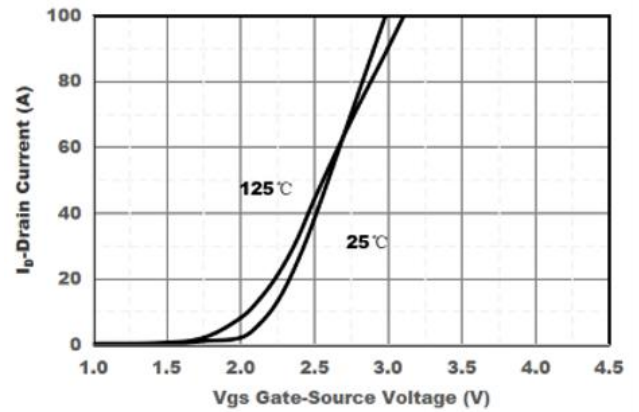


Figure2. Transfer Characteristics

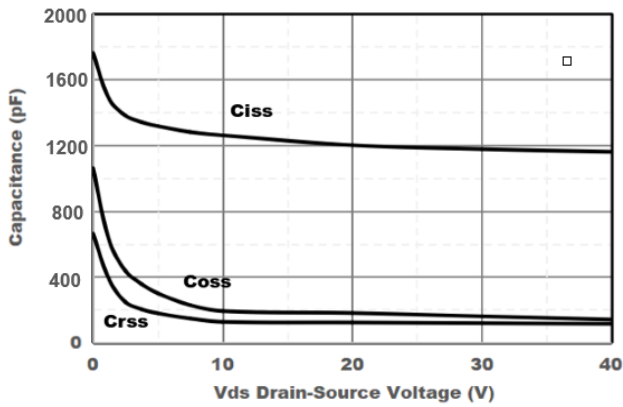


Figure3. Capacitance Characteristics

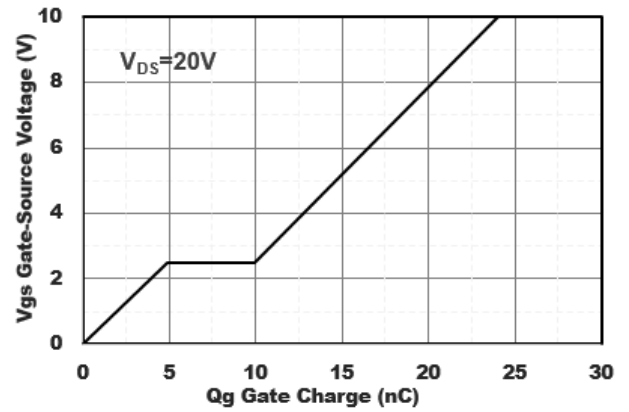


Figure4. Gate Charge

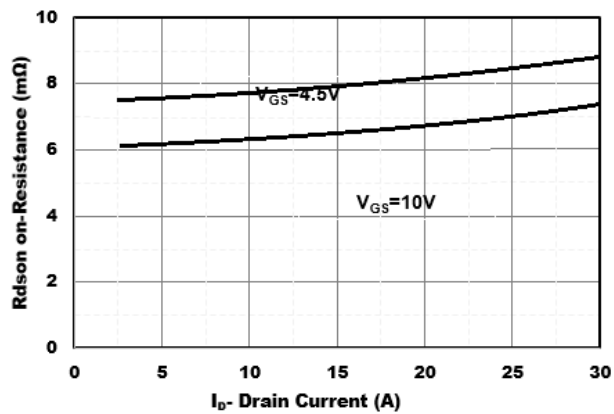


Figure5. Drain-Source on Resistance

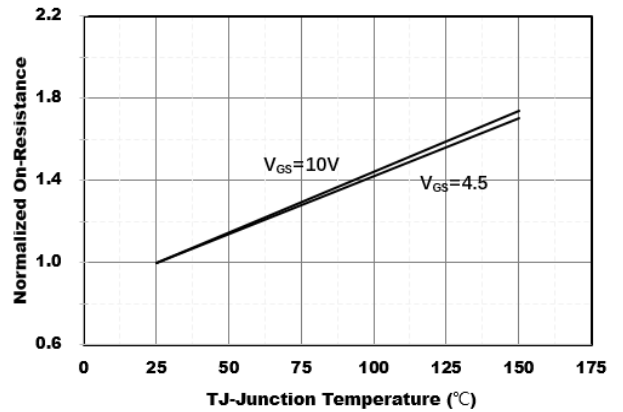


Figure6. Drain-Source on Resistance

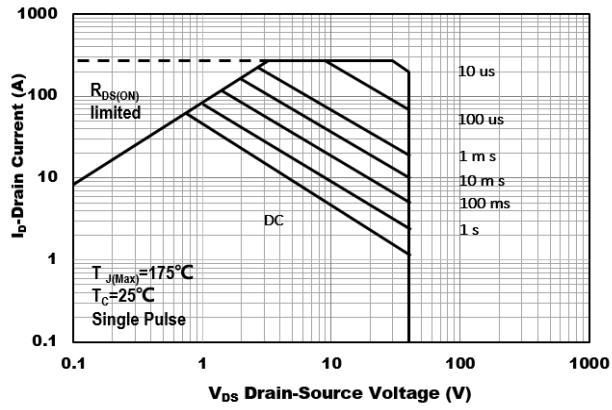


Figure7. Safe Operation Area

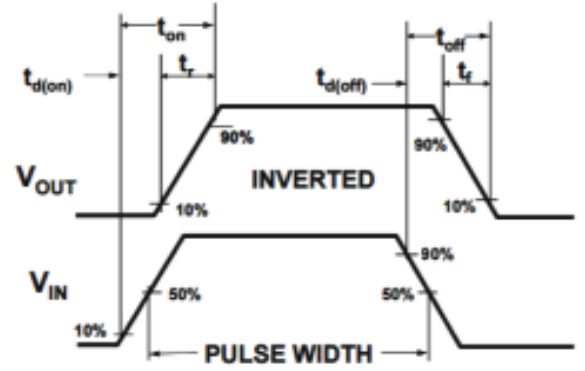
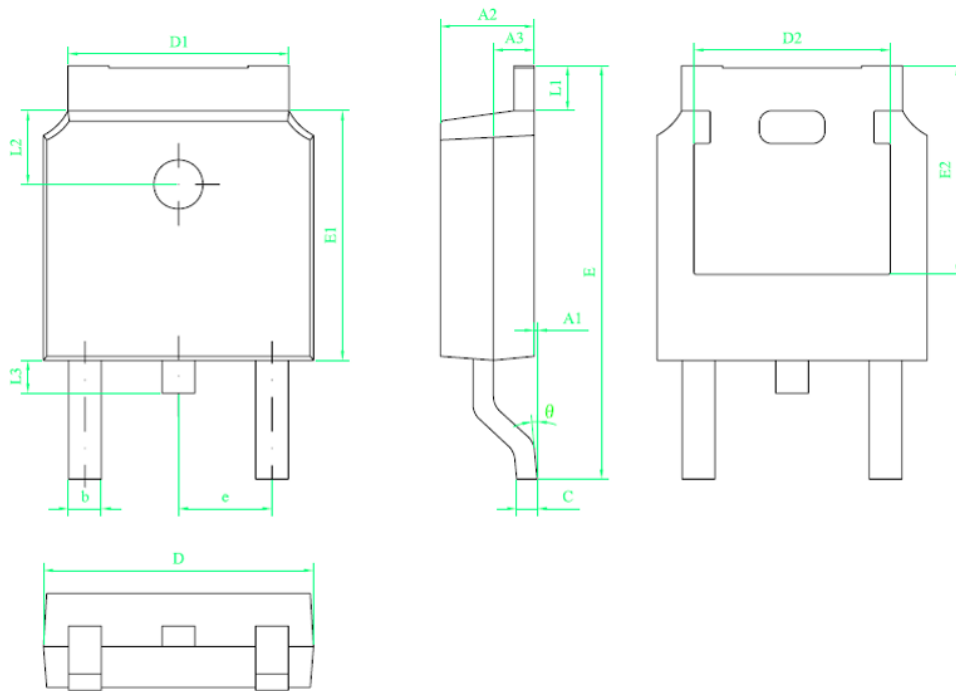


Figure8. Switching wave



YJD70N04A

■ TO-252 Package information



符 号	尺 寸		
	min	nom	max
A1	0	----	0.10
A2	2.20	2.30	2.40
A3	0.90	1.00	1.10
b	0.75	----	0.85
c	0.50	----	0.60
D	6.50	6.60	6.70
D1	5.30	5.40	5.50
D2	4.70	4.80	4.90
E	9.90	10.10	10.30
E1	6.00	6.10	6.20
E2	5.20	5.30	5.40
e	2.20	2.286	2.40
L1	0.90	----	1.25
L2	1.70	1.80	1.90
L3	0.60	0.80	1.00
θ	0°	----	8°

技术要求:

1. 树脂体不应有崩裂、缺损等缺陷;
2. 树脂上下部X、Y方向偏差不得超过0.20;
3. 胶体两端留胶总宽度和宽度不超过0.50;
4. 所有单位为mm;



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