U 3088 M · U 3089 M
U 3088 M – FP

8 SEGMENT INDICATOR DRIVER IN MICROCOMPUTER SYSTEMS

Technology: NCMOS, SI-GATE

Features:

- o 8 buffered, uncoded outputs, open drain, 15 mA each
- o Static drive of LED-indicators with common anode
- o Serial data-interface for software-controlled matching to the microcomputer
- o Pull-up-resistor at the inputs as a mask option (U 3089 M)

Case:

16-pin dual inline plastic (U 3088 M, U 3089 M)

16 pin SO plastic (U 3088 M-FP)

Absolute maximum ratings

Supply voltage	Pin 16	V_S	+7	V
Input voltages	Pin 2...5,15	V_I	-0.5 to V_S +0.5	V
	Pin 6...13	V_I	-0.5 to V_S +0.5	V
Output current (per pin)	Pin 6...13	I_O	50	mA
Power dissipation T_{amb} = 85 °C, T_j = 125 °C		P_{tot}	450	mW
Supply current		I_S	0.5	A
Junction temperature		T_j	125	°C
Ambient temperature range		T_{amb}	0 ... + 85	°C
Storage temperature range		T_{stg}	-25 ... + 125	°C

Maximum thermal resistance

Junction ambient		R_{thJA}	90	K/W

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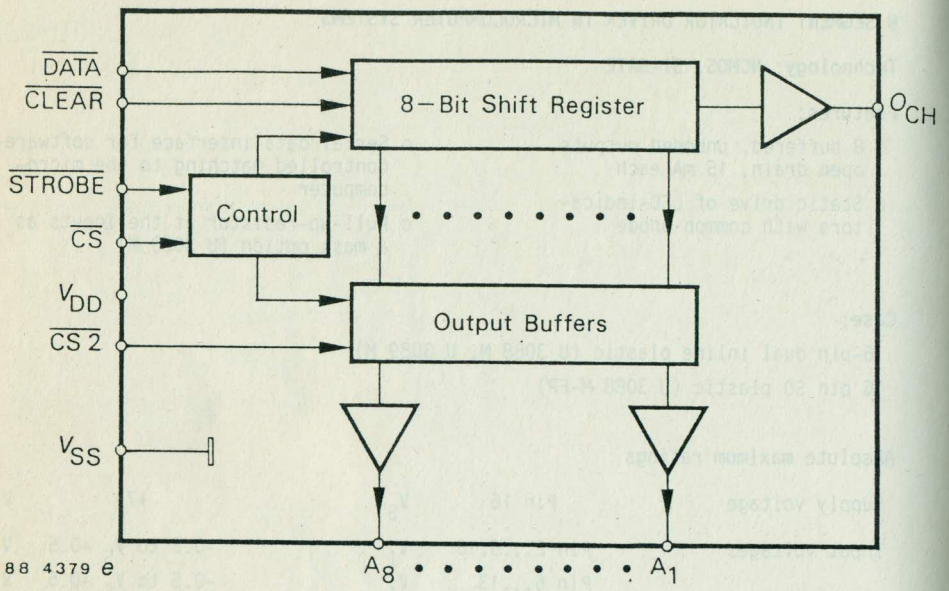

Fig. 1 Block diagram

Description

The U 3088 M is an output module in NCMOS, intended to be used primarily for the uncoded, static driving of LED-indicators. In addition to this use, the buffered outputs enable any desired peripheral function to be driven. In contrast with multiplexed driving circuits, the static outputs allow its use in television and radio sets without problems and free from interference.

The U 3088 M includes a 8-bit-shift-register with buffered outputs. This ensures that the outputs of the module do not change state uncontrolled when a new word is loaded.
An additional output of the shift register allows the cascading of several U 3088 M without additional circuitry. There is an asynchronous reset input for the shift register stages and an inhibit input for the outputs. $\overline{CLEAR}$ = LOW sets the register stages and inhibits all outputs (A1...A8 = HIGH). $\overline{CS2}$ = LOW also inhibits all outputs, but does not change the contents of the shift register.
The data interface for loading data into the U 3088 M is designed for simple, software-controlled matching with the I/O ports of microcomputers. The interface is enabled by $\overline{CS}$ = LOW. When $\overline{CS}$ is LOW, data bits can be transferred with the $\overline{STROBE}$ (active = LOW) from the data input into the shift register. At the same time $\overline{CS}$ = LOW halts the transfer from the shift register to the output buffer, so that the preceding information is held until $\overline{CS}$ goes HIGH.

Pin connection:

Pin	Function
1	Ground, 0 V
2	$\overline{DATA}$ Data input for the shift register. $\overline{DATA}$ = LOW switches the corresponding output to ground. The data bit lying on $\overline{DATA}$ is transferred with $\overline{STROBE}$ into position 19 (A19) of the shift register.
3	$\overline{STROBE}$ Clock pulse for shifting the information on lying on $\overline{DATA}$ into the shift register. The data bit currently on $\overline{DATA}$ is transferred into the internal shift register on the rising edge of $\overline{STROBE}$.
4	$\overline{CS}$ Chip Select. With $\overline{CS}$ = LOW the module is activated for the acceptance of a data-word and the output buffer is inhibited from accepting the new word. In the $\overline{CS}$ = LOW condition a data word can be written into the shift register with $\overline{STROBE}$ and $\overline{DATA}$. This requires the time t_{ST}. The transfer from the shift register to the output buffer takes place when $\overline{CS}$ changes from LOW to HIGH.
5	$\overline{CLEAR}$ Reset input. $\overline{CLEAR}$ = LOW sets all shift registers HIGH and inhibits all outputs. $\overline{CLEAR}$ may be asynchronous to clock and operates, if $\overline{CS}$ is active, until the rising edge of $\overline{CS}$ appears.
6...13	A 8 ... A 1 Open drain outputs, switching to ground on the corresponding $\overline{DATA}$ = LOW.
14	O_{CH} Shift register output. Allows cascading of several U 3088 M by connecting O_{CH} to the $\overline{DATA}$-input of the next U 3088 M.
15	$\overline{CS2}$ Output select. $\overline{CS2}$ = LOW inhibits all outputs to build a WIRED-OR connecting of several U 3088 M.
16	V_S Supply voltage +5 V ± 10 %

Electrical characteristics

V_S = 5 V, T_{amb} = 0...+85 °C,
reference point pin 1,
unless otherwise specified

		Min.	Typ.	Max.	
Supply voltage	V_S	4.5	5.0	5.5	V
Supply current (V_S = 5.5 V open outputs)	I_S			100	µA
Input voltage ($\overline{CS}$, $\overline{DATA}$, $\overline{STROBE}$)					
HIGH-level	V_{IH}	2.0		5.5	V
with pull-up-resistor	V_{IH}	2.0		5.5	V
LOW-level	V_{IL}			0.8	V
Input current (V_I = 5.5 V, without pull-up-resistor)	I_{IR}			10	µA
(V_I = 0 V, with pull-up-resistor)	I_{IL}			0.36	mA
Outputs (A1...A8) (Open drain)					
at I_{OL} = 1 mA	V_{OL}			0.4	V
at I_{OL} = 15 mA	V_{OL}			1	V
at V_O = 5.5 V	I_{OR}			50	µA
Switching time	t_O		1		µs

Switching characteristics ($\overline{CS}$, $\overline{DATA}$, $\overline{STROBE}$)

Chip Select to Strobe	t_{CSST}	1.0			µs
STROBE HIGH	t_{STH}	1.0			µs
STROBE LOW	t_{STL}	1.0			µs
STROBE	t_{ST}			100	µs
Data set	t_{DAS}	1.0			µs
Data hold	t_{DAH}	1.0			µs
End Chip Select to Strobe	t_{STCS}	1.0			µs

The times are referred to the levels:
LOW = 0.8 V
HIGH = 3.2 V

Timing diagrams

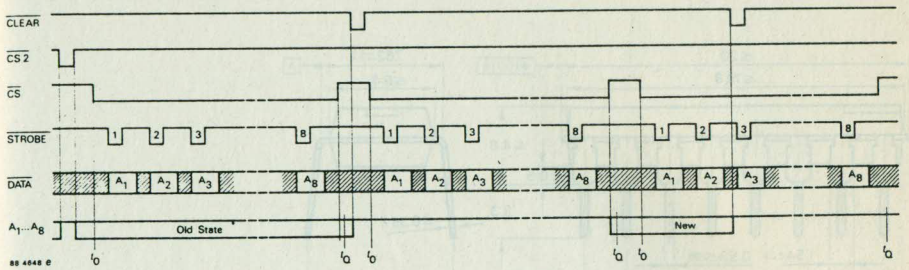

Fig. 2

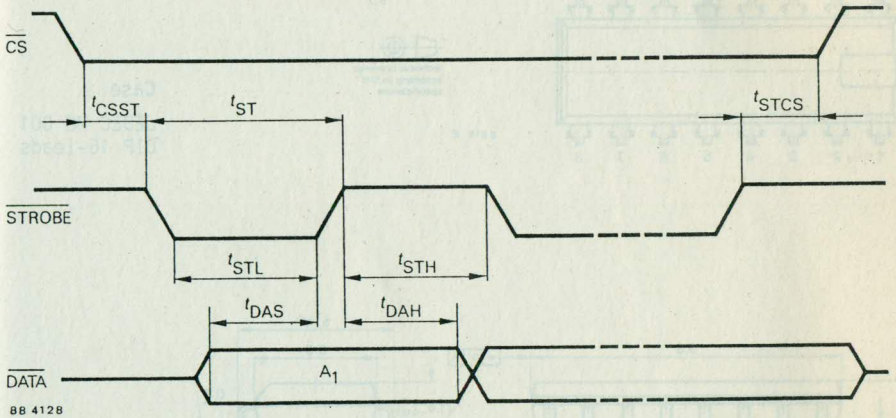

Fig. 3

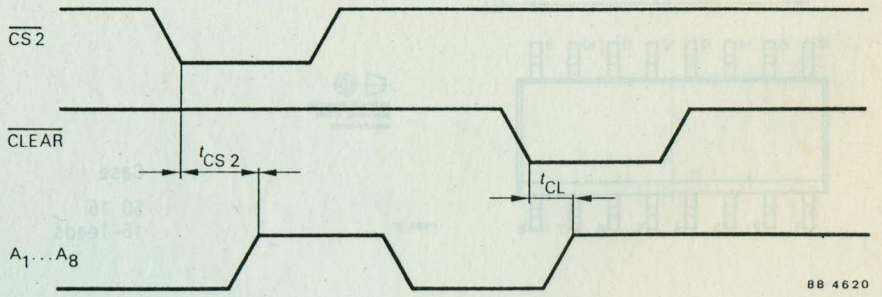

Fig. 4

U 3088 M · U 3089 M
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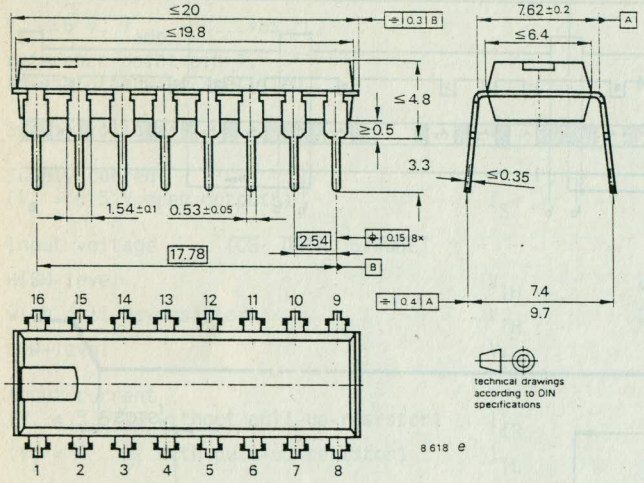
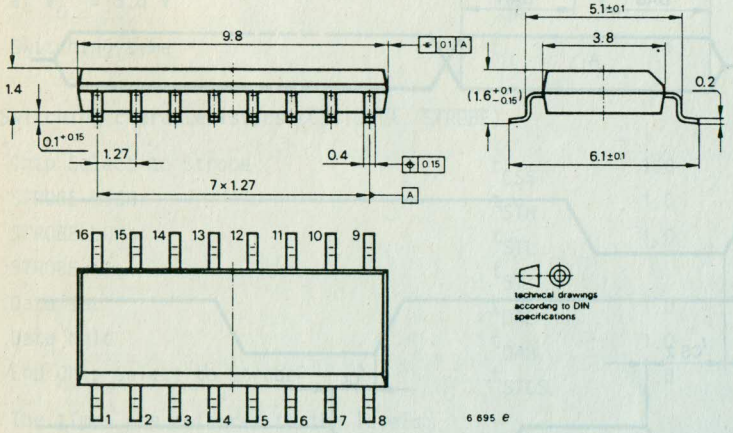
Dimensions in mm



Case

JEDEC MO 001
DIP 16-leads



Case

SO 16
16-leads