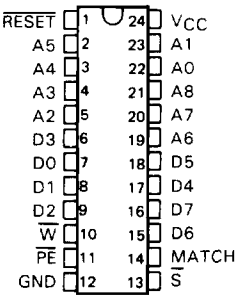
D2911, MARCH 1982 – REVISED SEPTEMBER 1985

- 'ACT2150A is Recommended for New Designs
- Fast Address to Match Valid Delay — Three Speed Ranges: 35 ns, 45 ns, 55 ns
- 512 × 9 Internal RAM
- 300-Mil 24-Pin Ceramic Side-Brazed or Plastic Dual-In-Line or Small Outline Packages
- Max Power Dissipation: 660 mW
- On-Chip Parity Generation and Checking
- Parity Error Output/Force Parity Error Input
- On-Chip Address/Data Comparator
- Asynchronous, Single-Cycle Reset
- Easily Expandable
- Fully Static
- Reliable SMOS (Scaled NMOS) Technology
- TTL- and CMOS Compatible Inputs and Outputs

DW, JD, OR NT PACKAGE
(TOP VIEW)



description

This 8-bit-slice cache address comparator consists of a high-speed 512 × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. It is fabricated using N-channel silicon gate technology for high speed and simple interface with MOS and bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be acheived with this device.

When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by the high level on the MATCH output. A low-level output from $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A $\overline{RESET}$ input is provided for initialization. When $\overline{RESET}$ goes low, all 512 × 9 RAM locations are cleared and the MATCH output is forced high.

The cache address comparator operates from a single 5-V supply and is offered in a 24-pin 300-mil ceramic side-brazed or plastic dual-in-line packages and plastic "Small Outline" packages. The device is fully TTL compatible and is characterized for operation from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\overline{RESET}$ = V_{IL},
or: $\overline{S}$ = V_{IH},
or: $\overline{W}$ = V_{IL}

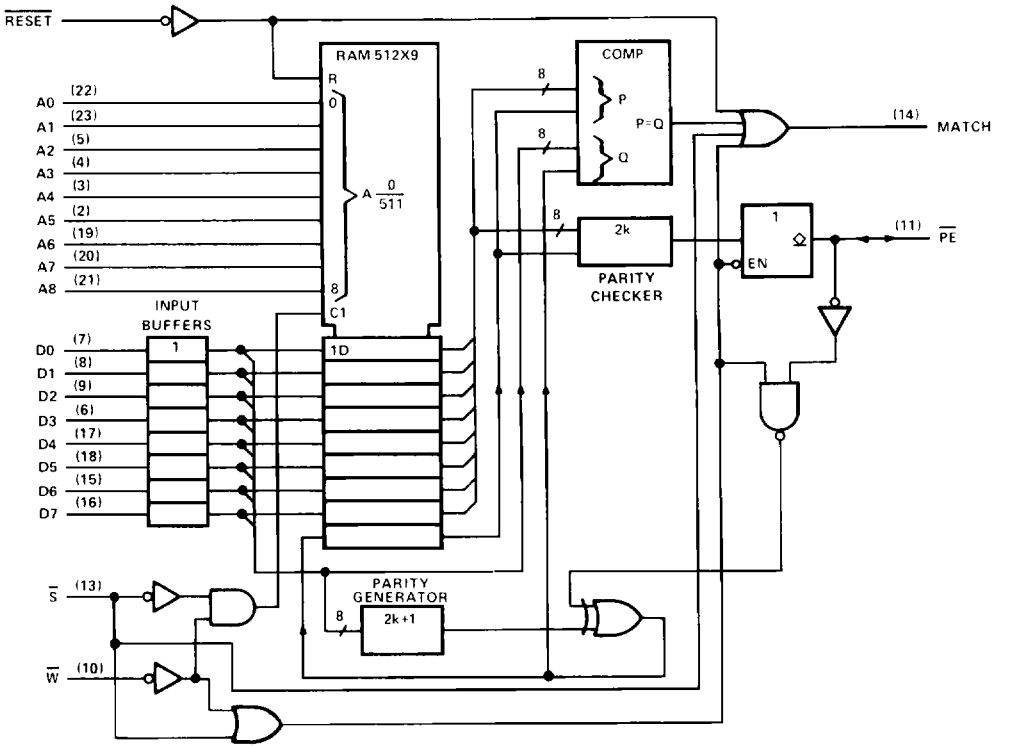
MATCH = V_{OL} if: [A0-A8] ≠ D0-D7 + parity,
with $\overline{RESET}$ = V_{IH},
$\overline{S}$ = V_{IL}, and $\overline{W}$ = V_{IH}

FUNCTION TABLE

OUTPUT		FUNCTION DESCRIPTION
MATCH	$\overline{PE}$	
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

Where S = V_{IL}, W = V_{IH}, RESET = V_{IH}

functional block diagram (positive logic)



This diagram has been changed to correct errors in previous versions. No functional change has been made in the chip.

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TERMINAL FUNCTIONS

PIN NAME	PIN NO.	DESCRIPTION
A0	22	Address inputs. Address 1 of 512-by-9-bit random-access memory locations. Must be stable for the duration of the write cycle.
A1	23	
A2	5	
A3	4	
A4	3	
A5	2	
A6	19	
A7	20	
A8	21	
D0	7	Data inputs. Compared with memory location addressed by A0-A8 when $\overline{W}$ is at V_{IH} and $\overline{S}$ is at V_{IL}. Provide input data to RAM when $\overline{W}$ is at V_{IL} and $\overline{S}$ is at V_{IL}.
D1	8	
D2	9	
D3	6	
D4	17	
D5	18	
D6	15	
D7	16	
GND	12	Ground
MATCH	14	When MATCH output is at V_{OH} during a compare cycle, D0 through D7 plus parity equal the contents of the 9-bit memory location addressed by A0 through A8.
$\overline{PE}$	11	Parity Error input/output. During write cycles, $\overline{PE}$ can force a parity error into the 9-bit location specified by A0 through A8 when $\overline{PE}$ is at V_{IL}. For compare cycles, $\overline{PE}$ at V_{OL} indicates a parity error in the stored data. $\overline{PE}$ is an open-drain output so an external pull-up resistor is required.
$\overline{RESET}$	1	$\overline{RESET}$ input. Asynchronously clears entire RAM array and forces MATCH high when $\overline{RESET}$ is at V_{IL} and $\overline{W}$ is at V_{IH}.
$\overline{S}$	13	Chip select input. Enables device when $\overline{S}$ is at V_{IL}. Deselects device and forces MATCH high when $\overline{S}$ is at V_{IH}.
V_{CC}	24	5-V supply voltage
$\overline{W}$	10	Write control input. Writes D0 through D7 and generated parity into RAM and forces MATCH high when $\overline{W}$ is at V_{IL} and $\overline{S}$ is at V_{IL}. Places selected device in compare mode if $\overline{W}$ is at V_{IH}.

absolute maximum ratings over operating free-air temperature range (unless otherwise specified)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −1.5 V to 7 V
Input voltage range, any input . . . . . −1.5 V to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated condtions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		6	V
V_{IL}	Low-level input voltage (See Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS2150-3		TMS2150-4 TMS2150-5		UNIT
			MIN	MAX	MIN	MAX	
$V_{OH(M)}$	MATCH high-level output voltage	V_{CC} = 4.5 V, I_{OH} = −2 mA	2.4		2.4		V
		V_{CC} = 4.5 V, I_{OH} = −20 μA	3.5		3.5		
$V_{OL(M)}$	MATCH low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 4 mA		0.4		0.4	V
$V_{OL(PE)}$	$\overline{PE}$ low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 12 mA		0.4		0.4	V
I_I	Input current	V_I = 0 V to 5.5 V		10		10	μA
$I_{OL(PE)}$	$\overline{PE}$ output sink current	V_{CC} = 4.5 V, V_{OL} = 0.4 V	12		12		mA
I_{OS}‡	Short-circuit MATCH output current	V_{CC} = 5.5 V, V_O = GND		−150		−150	mA
I_{CC1}	Supply current (operative)	$\overline{RESET}$ = V_{IH}		145		135	mA
I_{CC2}	Supply current (reset)	$\overline{RESET}$ = V_{IL}		155		145	mA
C_i	Input capacitance	V_I = 0 V, f = 1 MHz		5		5	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		6		6	pF

‡Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature†

PARAMETER		TMS2150-3		TMS2150-4		TMS2150-5		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address to MATCH		35		45		55	ns
$t_{a(A-P)}$	Access time from address to $\overline{PE}$		45		55		65	ns
$t_{a(S)}$	Access time from $\overline{S}$ to MATCH		20		25		35	ns
$t_{p(D)}$	Propagation time, data inputs to MATCH		20		35		45	ns
$t_{p(R-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high		30		30		40	ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high		20		25		35	ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high		20		25		35	ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high		20		25		35	ns
$t_{v(A)}$	MATCH valid time after change of address	5		5		5		ns
$t_{v(A-P)}$	$\overline{PE}$ valid time after change of address	15		15		15		ns

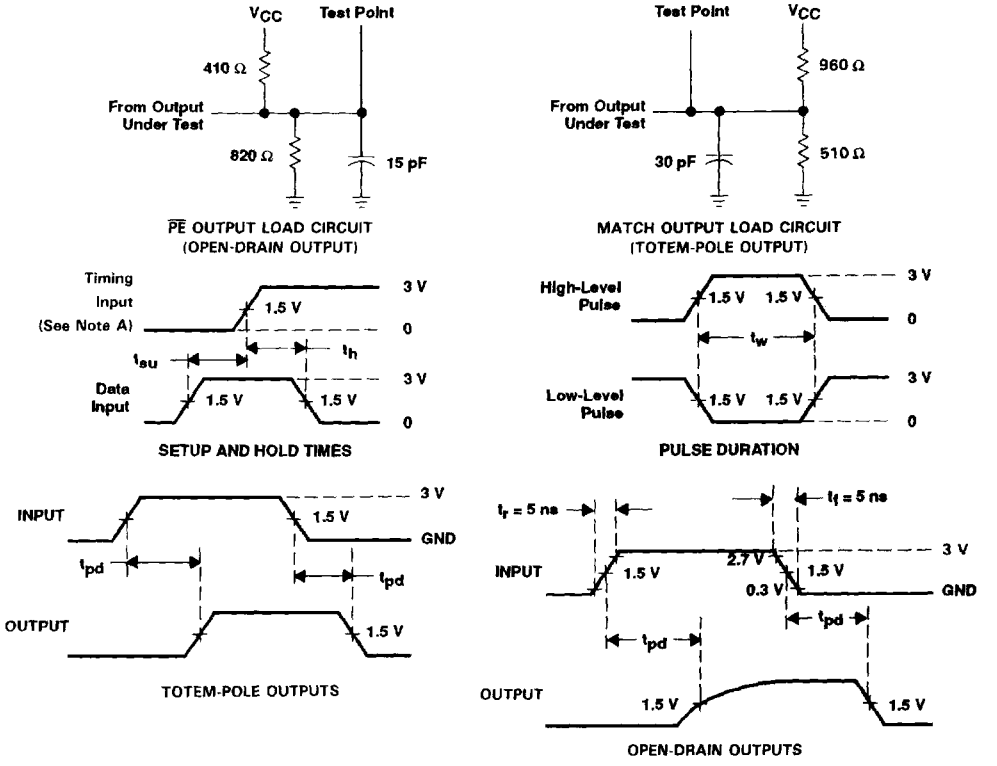
†See Parameter Measurement Information for load circuits and voltage waveforms.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS2150-3		TMS2150-4		TMS2150-5		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time, without writing $\overline{PE}$	30		40		50		ns
$t_{cPE(W)}$	Write cycle time, writing $\overline{PE}$ (see Note 3)	35		40		50		ns
$t_{c(rd)}$	Read cycle time	35		45		55		ns
$t_{w(RL)}$	Pulse duration, $\overline{RESET}$ low	35		35		45		ns
$t_{(WL)}$	Pulse duration $\overline{W}$ low, without writing $\overline{PE}$	20		25		30		ns
$t_{wPE(WL)}$	Pulse duration, $\overline{W}$ low, writing $\overline{PE}$ (see Note 3)	35		40		45		ns
$t_{su(A)}$	Address setup time before $\overline{W}$ low	0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ high	20		25		30		ns
$t_{su(P)}$	$\overline{PE}$ setup time before $\overline{W}$ high (see Note 3)	20		25		30		ns
$t_{su(S)}$	Chip select setup time before $\overline{W}$ high	20		25		30		ns
$t_{su(RH)}$	$\overline{RESET}$ inactive setup time before first tag cycle	0		0		0		ns
$t_{h(A)}$	Address hold time after $\overline{W}$ high	0		0		5		ns
$t_{h(D)}$	Data hold time after $\overline{W}$ high	5		5		10		ns
$t_{h(P)}$	$\overline{PE}$ hold time after $\overline{W}$ high	0		0		5		ns
$t_{h(S)}$	Chip select hold time after $\overline{W}$ high	0		0		0		ns
t_{AVWH}	Address valid to write enable high	30		40		50		ns

NOTE 3: Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle time when writing a parity error, $t_{cPE(W)}$.

PARAMETER MEASUREMENT INFORMATION



NOTE A: Input rise and fall times are 5 ns.

FIGURE 1. TIMING REFERENCE LEVELS

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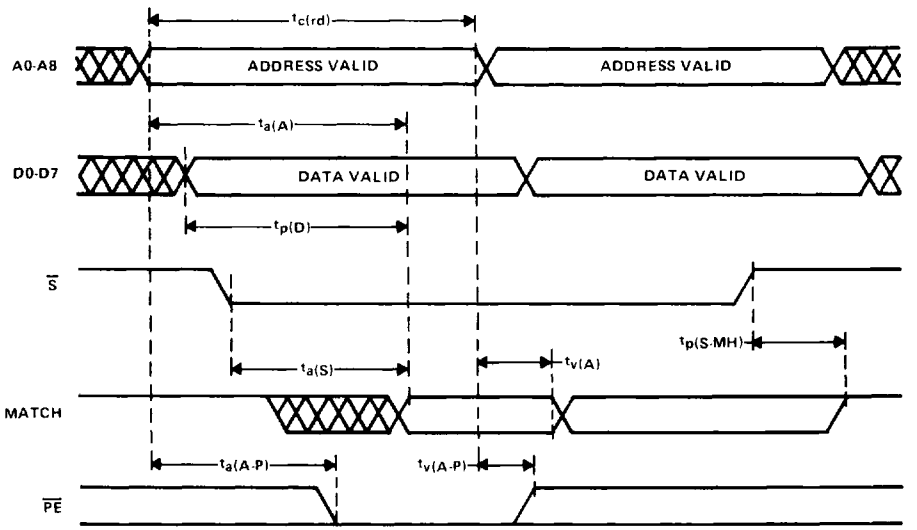
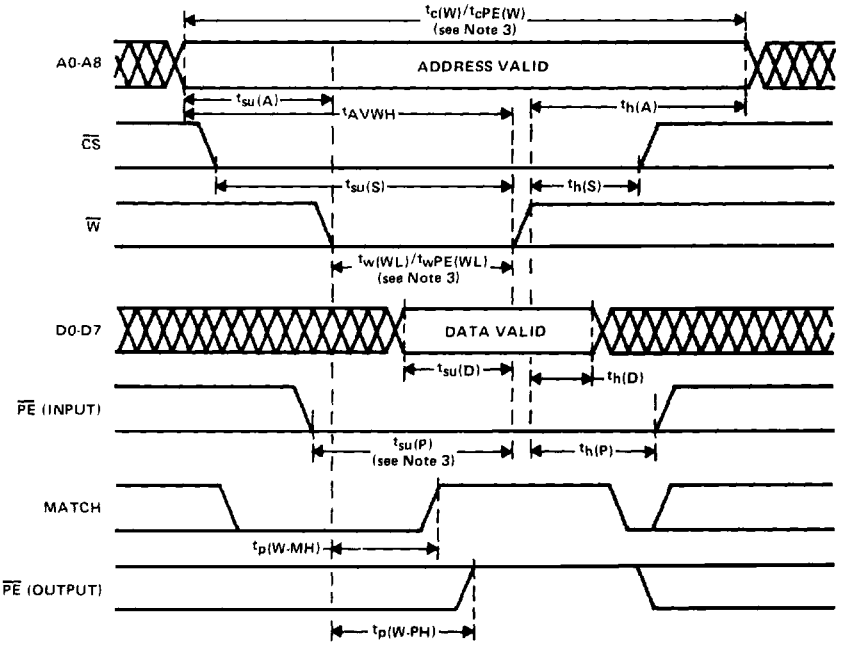
PARAMETER MEASUREMENT INFORMATION



NOTE: Input pulse levels are 0 V and 3 V, with rise and fall times of 5 ns. The timing reference levels on the input pulses are 0.8 V and 2 V. The timing reference level for output pulses is 1.5 V.

FIGURE 2. COMPARE CYCLE TIMING

PARAMETER MEASUREMENT INFORMATION



NOTE 3: Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle time when writing a parity error, $t_{cPE(W)}$.

FIGURE 3. WRITE CYCLE TIMING

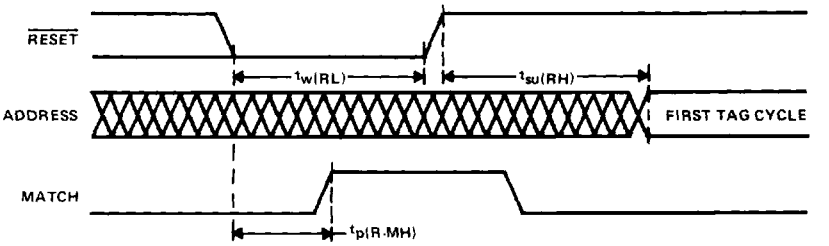


FIGURE 4. RESET CYCLE TIMING