

TLP113

ISOLATED LINE RECEIVER

SIMPLEX/MULTIPLEX DATA TRANSMISSION

COMPUTER-PERIPHERAL INTERFACE

MICROPROCESSOR SYSTEM INTERFACE

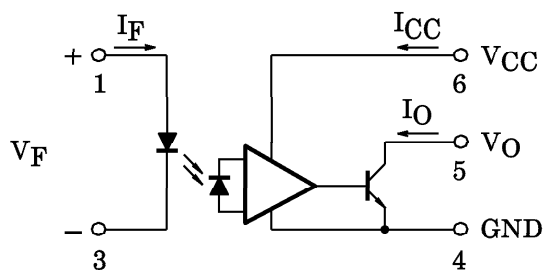
DIGITAL ISOLATION FOR A/D, D/A CONVERSION

The TOSHIBA MINI FLAT COUPLER TLP113 is a small outline coupler, suitable for surface mount assembly.

TLP113 consists of a GaAlAs light emitting diode, optically coupled to an integrated high gain, high speed photodetector whose output is an open collector, schottky clamped transistor.

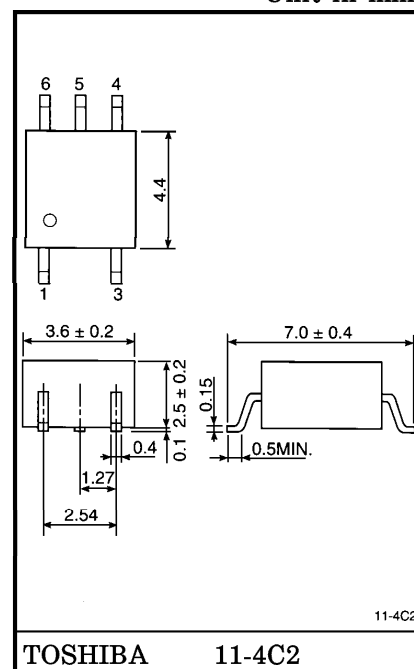
- Input Current Thresholds : $I_F = 10\text{mA}$ (Max.)
- Switching Speed : 10MBd (Typ.)
- TTL / LSTTL Compatible : $V_{CC} = 5\text{V}$
- Guaranteed Performance Over Temp. : $0 \sim 70^\circ\text{C}$
- Isolation Voltage : 2500Vrms (Min.)
- UL Recognized : UL1577 File No. E67349

SCHEMATIC



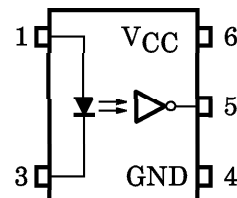
(Note) A $0.1\mu\text{F}$ bypass capacitor must be connected between pins 4 and 6.

Unit in mm



Weight : 0.09g

PIN CONFIGURATION (TOP VIEW)



- 1 : ANODE
 3 : CATHODE
 4 : GND
 5 : OUTPUT
 (OPEN COLLECTOR)
 6 : V_{CC}

TRUTH TABLE (Positive Logic)

INPUT	OUTPUT
H	L
L	H

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current	I _F	20	mA
	Pulse Forward Current (Note 1)	I _{FP}	40	mA
	Peak Transient Forward Current (Note 2)	I _{FPT}	1	A
	Reverse Voltage	V _R	5	V
DETECTOR	Output Current	I _O	25	mA
	Output Voltage	V _O	7	V
	Supply Voltage (1 Minute Maximum)	V _{CC}	7	V
	Output Power Dissipation	P _o	40	mW
Operating Temperature Range		T _{opr}	−40~85	°C
Storage Temperature Range		T _{stg}	−55~125	°C
Lead Solder Temperature (10s)		T _{sol}	260	°C
Isolation Voltage (AC, 1 min., RH ≤ 60%, Note 4)		BV _S	2500	V _{rms}

(Note 1) 50% duty cycle, 1ms pulse width.

(Note 2) Pulse width ≤ 1μs, 300pps.

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Voltage, Low Level	V _{FL}	−3	0	1.0	V
Input Current, High Level	I _{FH}	13 *	16	20	mA
Supply Voltage	V _{CC}	4.5	5	5.5	V
Fan Out (TTL Load, Each Channel)	N	—	—	8	—
Operating Temperature	T _{opr}	0	—	70	°C

* 13mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 10mA or less.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 4.5 \sim 5.5\text{V}$, $V_{FL} \leq 1.0\text{V}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Forward Voltage	V_F	$I_F = 10\text{mA}$, $T_a = 25^\circ\text{C}$	—	1.65	1.80	V
Forward Voltage Temperature Coefficient	V_F / T_a	$I_F = 10\text{mA}$	—	-2	—	mV / $^\circ\text{C}$
Reverse Current	I_R	$V_R = 5\text{V}$, $T_a = 25^\circ\text{C}$	—	—	10	μA
Capacitance Between Terminals	C_T	$V_F = 0$, $f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$	—	45	—	pF
High Level Output Current	I_{OH}	$V_F = 1.0$, $V_O = 5.5\text{V}$	—	—	250	μA
		$V_F = 1.0$, $V_O = 5.5\text{V}$, $T_a = 25^\circ\text{C}$	—	0.5	10	
Low Level Output Voltage	V_{OL}	$I_F = 10\text{mA}$ $I_{OL} = 13\text{mA}$ (Sinking)	—	0.4	0.6	V
“H Level Output→L Level Output” Input Current	I_{FH}	$I_{OL} = 13\text{mA}$ (Sinking) $V_{OL} = 0.6\text{V}$	—	—	10	mA
High Level Supply Current	I_{CCH}	$V_{CC} = 5.5\text{V}$, $I_F = 0$	—	7	15	mA
Low Level Supply Current	I_{CCL}	$V_{CC} = 5.5\text{V}$, $I_F = 16\text{mA}$	—	12	18	mA
Input-Output Insulation Leakage Current	I_S	$V_S = 3540\text{V}$, $t = 5\text{s}$ $T_a = 25^\circ\text{C}$ (Note 4)	—	—	100	μA
Isolation Resistance	R_S	$R.H. \leq 60\%$, $V_S = 500\text{V DC}$ $T_a = 25^\circ\text{C}$ (Note 4)	5×10^{10}	10^{14}	—	Ω
Stray Capacitance Between Input to Output	C_S	$V_S = 0$, $f = 1\text{MHz}$ $T_a = 25^\circ\text{C}$ (Note 4)	—	0.8	—	pF

* All typical values are $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^\circ C$)

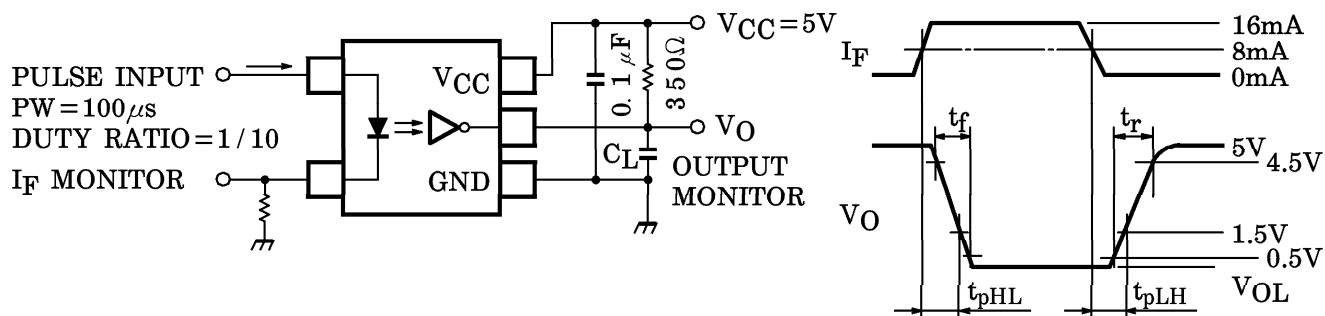
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (H $\rightarrow$ L)	t_{pHL}	1	$I_F = 0 \rightarrow 16mA$ $C_L = 15pF$, $R_L = 350\Omega$	—	60	120	ns
Propagation Delay Time (L $\rightarrow$ H)	t_{pLH}	1	$I_F = 16 \rightarrow 0mA$ $C_L = 15pF$, $R_L = 350\Omega$	—	60	120	ns
Output Rise-Fall Time (10-90%)	t_r , t_f	2	$R_L = 350\Omega$, $C_L = 15pF$ $I_F = 0 \rightleftharpoons 16mA$	—	30	—	ns
Common Mode Transient Immunity at High Output Level	CM_H	2	$I_F = 0mA$, $V_{CM} = 200V_{p-p}$ $V_{O(MIN)} = 2V$, $R_L = 350\Omega$	—	200	—	V / μs
Common Mode Transient Immunity at Low Output Level	CM_L	2	$I_F = 16mA$, $V_{CM} = 200V_{p-p}$ $V_{O(MAX)} = 0.8V$, $R_L = 350\Omega$	—	-500	—	V / μs

(Note 4) Device considered a two-terminal device : Pins 1 and 3 shorted together, and pins 4, 5 and 6 shorted together.

(Note 5) The V_{CC} supply voltage to each TLP113 isolator must be bypassed by $0.1\mu F$ capacitor, This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to package V_{CC} and GND pins of each device.

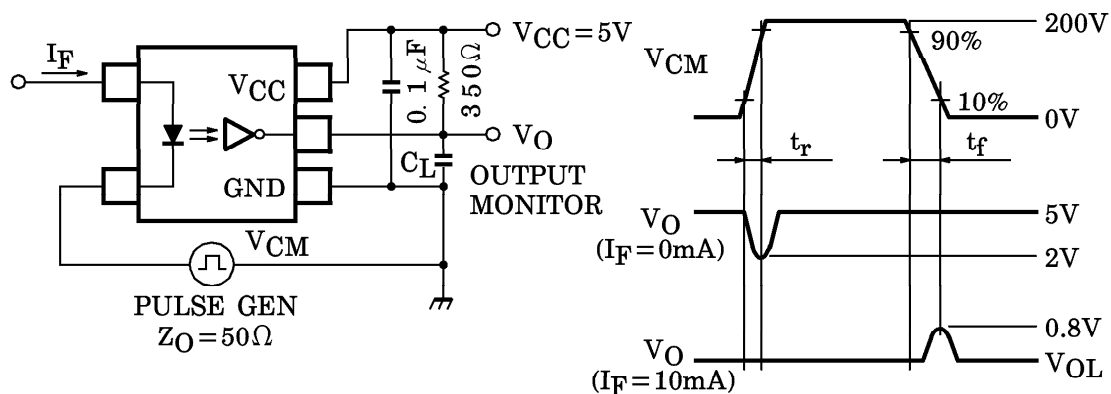
(Note 6) Maximum electrostatic discharge voltage for any pins : 180V (C=200pF, R=0)

TEST CIRCUIT 1 : Switching Time Test Circuit



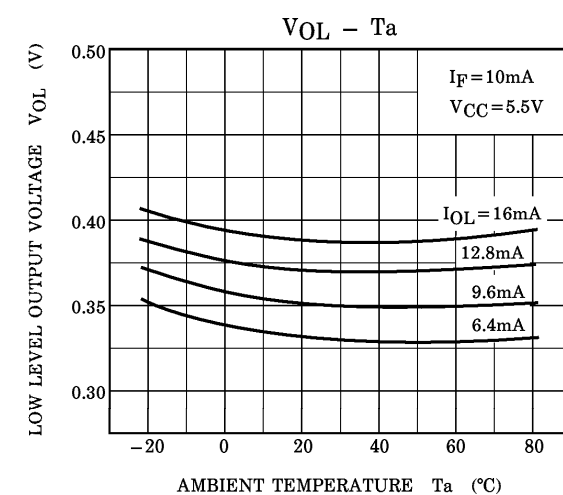
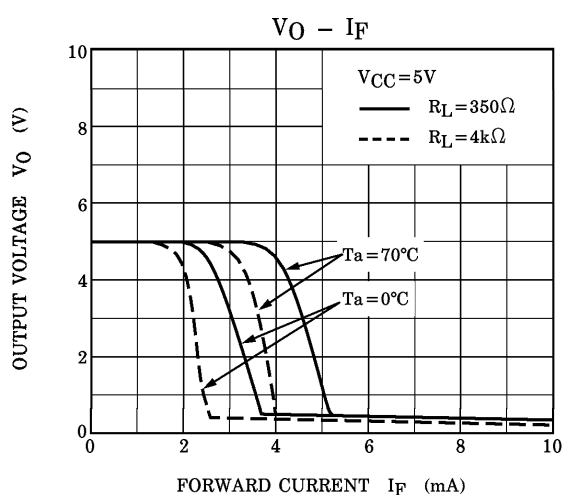
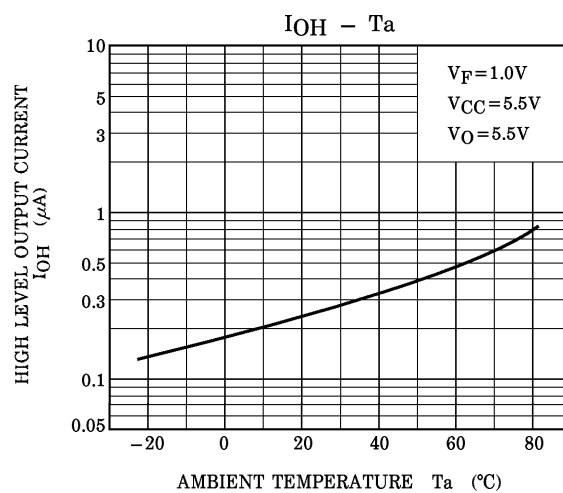
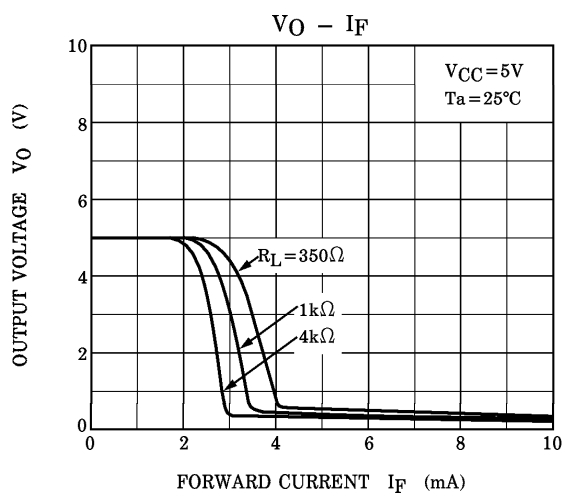
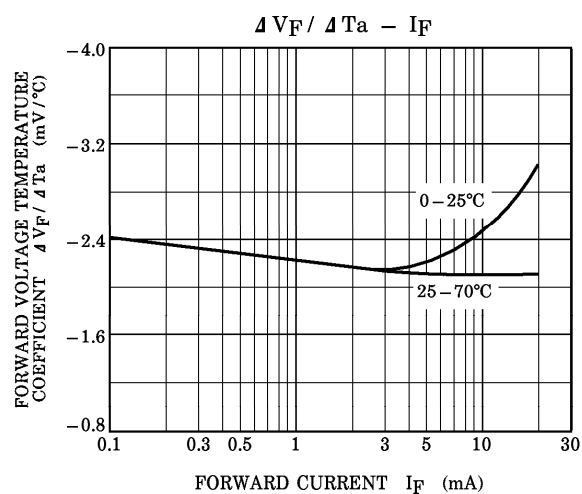
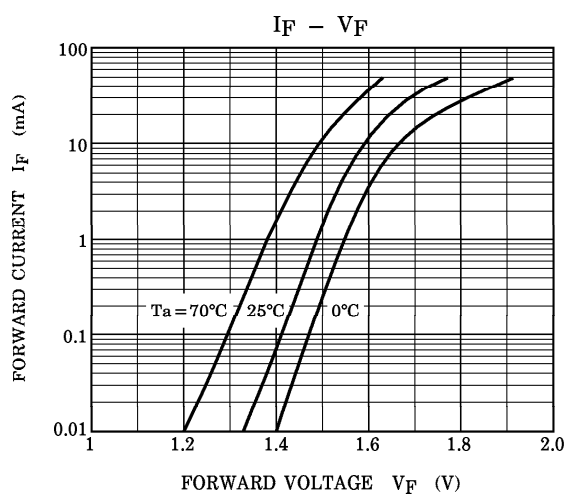
C_L is approximately 15pF which includes probe and stray wiring capacitance.

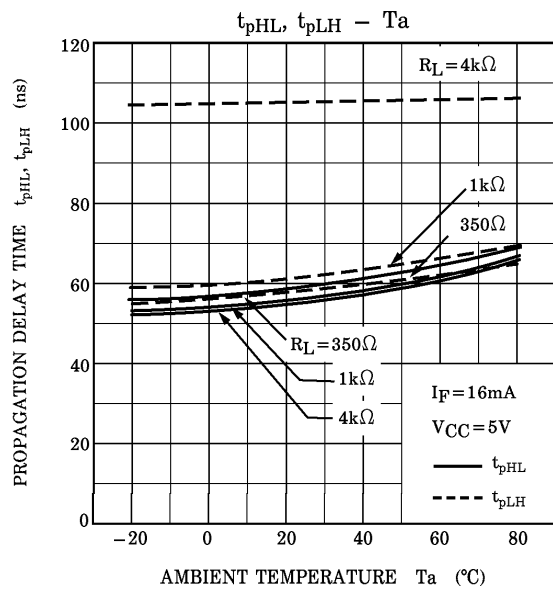
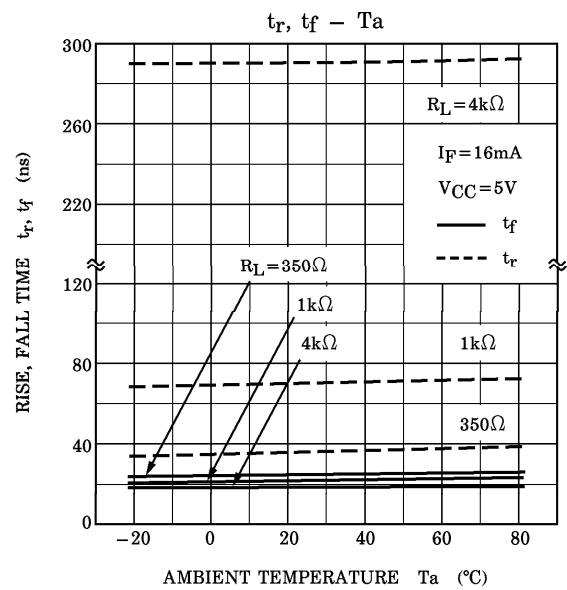
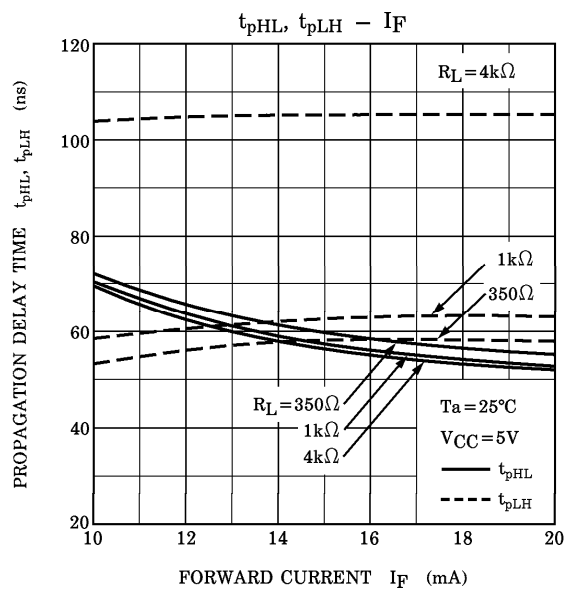
TEST CIRCUIT 2 : Common Mode Transient Immunity Test Circuit



$$CM_H = \frac{160(V)}{t_r(\mu s)}, CM_L = \frac{160(V)}{t_f(\mu s)}$$

C_L is approximately 15pF which includes probe and stray wiring capacitance.





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