SN74LVC1G3157 Single-Pole Double-Throw Analog Switch

1 Features

- ESD protection exceeds JESD 22
  - 2000V Human Body Model (A114-A)
  - 1000V Charged-Device Model (C101)
- 1.65V to 5.5V V_{CC} operation
- Qualified for 125°C operation
- Specified break-before-make switching
- Rail-to-rail signal handling
- Operating frequency typically 340MHz at room temperature
- High speed, typically 0.5ns (V_{CC} = 3V, C_L = 50pF)
- Low ON-state resistance, typically approximately 6Ω (V_{CC} = 4.5V)
- Latch-up performance exceeds 100mA Per JESD 78, class II

2 Applications

- Wearables and mobile devices
- Portable computing
- Internet of things (IoT)
- Audio signal routing
- Remote radio unit
- Portable medical equipment
- Surveillance
- Home automation
- I2C/SPI/UART bus multiplexing
- Wireless charging

3 Description

This single channel single-pole double-throw (SPDT) analog switch is designed for 1.65V to 5.5V V_{CC} operation.

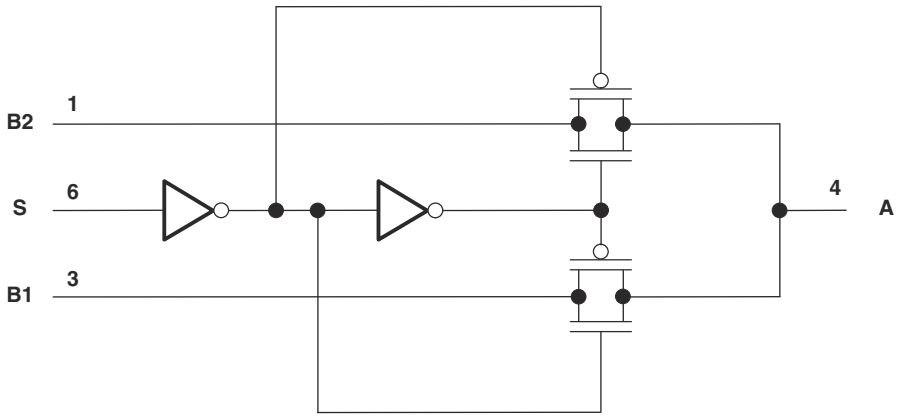
The SN74LVC1G3157 device handles both analog and digital signals. The SN74LVC1G3157 device allows signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
SN74LVC1G3157	SOT-23 (DBV) (6)	2.90mm × 1.60mm
	SC70 (DCK) (6)	2.00mm × 1.25mm
	SOT (DRL) (6)	1.60mm × 1.20mm
	SON (DRY) (6)	1.45mm × 1.00mm
	DSBGA (YZP) (6)	1.41mm × 0.91mm
	SON (DSF) (6)	1.00mm × 1.00mm
	X2SON (DTB) (6)	0.80mm × 1.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

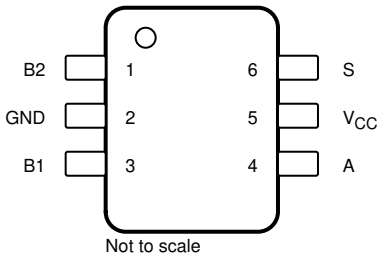

Figure 4-1. DBV Package, 6-Pin SOT-23 (Top View)

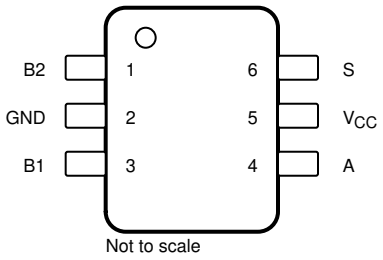

Figure 4-2. DCK Package, 6-Pin SC70 (Top View)

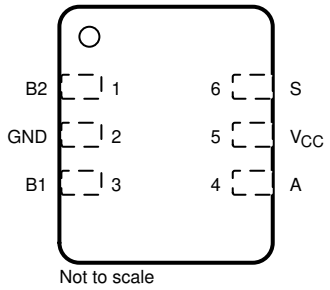

Figure 4-3. DRY Package, 6-Pin SON (Top View)

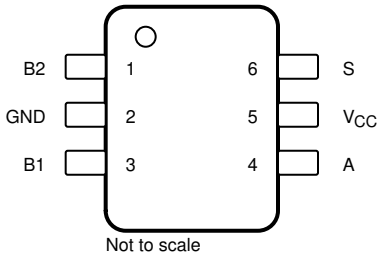

Figure 4-4. DRL Package, 6-Pin SOT (Top View)

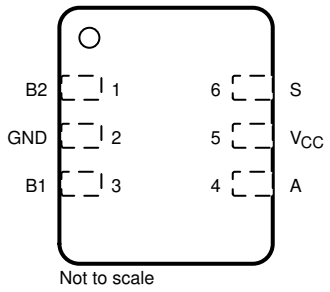

Figure 4-5. DSF Package, 6-Pin SON (Top View)

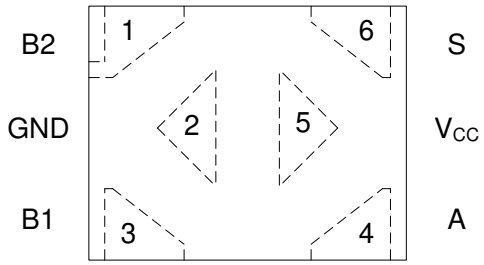

Figure 4-6. DTB Package, 6-Pin X2SON (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	SOT-23, SC70, SON, X2SON, or SOT		
B2	1	I/O	Switch I/O. Set S high to enable.
GND	2	P	Ground
B1	3	I/O	Switch I/O. Set S low to enable.
A	4	I/O	Common terminal
V_{CC}	5	P	Power supply
S	6	I	Select

(1) I = input, O = output, P = power

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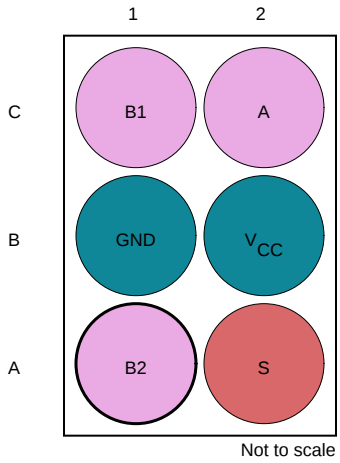

Figure 4-7. YZP Package, 6-Pin DSBGA (Bottom View)

Legend	
Input	Input or Output
Power	

Table 4-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
A1	B2	I/O	Switch I/O. Set S high to enable.
A2	S	I	Select
B1	GND	P	Ground
B2	V_{CC}	P	Power supply
C1	B1	I/O	Switch I/O. Set S low to enable.
C2	A	I/O	Common terminal

(1) I = input, O = output, P = power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	(YZP, DSF. DTB. DRY, DRL) Supply voltage(2)	-0.5	6.5	V
V_{CC}	(DBV, DCK) Supply voltage(2)	-0.5	6	V
V_{IN}	(YZP, DSF. DTB. DRY, DRL) Control input voltage(2) (3)	-0.5	6.5	V
V_{IN}	(DBV, DCK) Control input voltage(2) (3)	-0.5	6	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4) (5)	-0.5	V_{CC} + 0.5V	V
I_{IK}	Control input clamp current V_{IN} < 0	-50		mA
$I_{I/OK}$	I/O port diode current $V_{I/O}$ < 0 or $V_{I/O}$ > V_{CC}	-50	50	mA
$I_{I/O}$	On-state switch current(6) $V_{I/O}$ = 0 to V_{CC}	-128	128	mA
	Continuous current through V_{CC} or GND	-100	100	mA
T_J	Junction temperature		150	C
T_{stg}	Storage temperature	-65	150	C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) V_I, V_O, V_A, and V_{Bn} are used to denote specific conditions for $V_{I/O}$.
(6) I_I, I_O, I_A, and I_{Bn} are used to denote specific conditions for $I_{I/O}$.

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5.2 Thermal Information

THERMAL METRIC		SN74LVC1G3157						UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (SON)	DTB (X2SON)	YZP (DSBGA)	
		6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	258.2	286.4	244.1	284.2	324.5	129.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	182.8	224.6	112.5	138.6	150.5	1.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	142.8	143.7	109.9	170.9	239.0	40.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	118.4	124.5	9.3	13.7	17.2	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	142.2	142.8	109.3	167.9	238.3	40.2	°C/W

5.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		1.65		5.5	V
$V_{I/O}$	Switch input or output voltage (Max of V_{CC})		0		V_{CC}	V
V_{IN}	Control input voltage		0		5.5	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65V to 1.95V	V_{CC} * 0.75			V
		V_{CC} = 2.3V to 5.5V	V_{CC} * 0.7			V
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65V to 1.95V			V_{CC} * 0.25	V
		V_{CC} = 2.3V to 5.5V			V_{CC} * 0.3	V
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8 ± 0.15V			20	ns/V
		V_{CC} = 2.5 ± 0.2V			20	
		V_{CC} = 3.3V ± 0.3V			10	
		V_{CC} = 5V ± 0.5V			10	
T_A	Operating free-air temperature	BGA package (YZP)	-40		85	°C
		All other packages (DBV, DCK, DRL, DRY, DSF)	-40		125	

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation. See the TI application report, Implications of Slow or Floating CMOS Inputs (SCBA004)

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5.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
SN74LVC1G3157									
		V_{CC} V	$V_{I/O}$ V	I_O mA	T_A				
r_{ON}	ON-state switch resistance[2]	1.65	V_I = 0 V	I_O = 4 mA	25°C		11		Ω
					–40°C to +85°C			20	
					–40°C to +125°C			20	
			V_I = 1.65	I_O = -4 mA	25°C		15		
					–40°C to +85°C			50	
					–40°C to +125°C			50	
		2.3	V_I = 0 V	I_O = 8 mA	25°C		8		
					–40°C to +85°C			12	
					–40°C to +125°C			12	
			V_I = 2.3 V	I_O = -8 mA	25°C		11		
					–40°C to +85°C			30	
					–40°C to +125°C			30	
		3	V_I = 0 V	I_O = 24 mA	25°C		7		
					–40°C to +85°C			9	
					–40°C to +125°C			9	
			V_I = 3 V	I_O = -24 mA	25°C		9		
					–40°C to +85°C			20	
					–40°C to +125°C			20	
		4.5	V_I = 0 V	I_O = 30 mA	25°C		6		
					–40°C to +85°C			7	
					–40°C to +125°C			7	
			V_I = 2.4 V	I_O = 30 mA	25°C		7		
					–40°C to +85°C			12	
					–40°C to +125°C			12	
			V_I = 4.5 V	I_O = -30 mA	25°C		7		
					–40°C to +85°C			15	
					–40°C to +125°C			15	
r_{range}	(YZP, DSF. DTB. DRY, DRL) ON-state switch resistance over signal range[2] [3]	1.65	0 ≤ V_{Bn} ≤ V_{CC}	I_A = -4 mA	25°C			140	Ω
					–40°C to +85°C			140	
					–40°C to +125°C			140	
		2.3		I_A = -8 mA	25°C			45	
					–40°C to +85°C			45	
					–40°C to +125°C			45	
		3		I_A = -24 mA	25°C			18	
					–40°C to +85°C			18	
					–40°C to +125°C			18	
		4.5		I_A = -30 mA	25°C			10	
					–40°C to +85°C			10	
					–40°C to +125°C			10	

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Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
r_{range}	(DBV, DCK) ON-state switch resistance over signal range(2) (3)	1.65	0 ≤ V_{Bn} ≤ V_{CC}	I_A = -4 mA	25°C			200	Ω
					–40°C to +85°C			200	
					–40°C to +125°C			200	
		2.3		I_A = -8 mA	25°C			65	
					–40°C to +85°C			65	
					–40°C to +125°C			65	
		3		I_A = -24 mA	25°C			25	
					–40°C to +85°C			25	
					–40°C to +125°C			25	
		4.5		I_A = -30 mA	25°C			15	
					–40°C to +85°C			15	
					–40°C to +125°C			15	
Δr_{ON}	Maximum ON resistance between any two channels (2) (4) (5)	1.65	V_{Bn} = 1.15 V	I_A = -4 mA	25°C		0.5		Ω
					–40°C to +85°C		0.5		
					–40°C to +125°C		0.5		
		2.3	V_{Bn} = 1.6 V	I_A = -8 mA	25°C		0.1		
					–40°C to +85°C		0.1		
					–40°C to +125°C		0.3		
		3	V_{Bn} = 2.1 V	I_A = -24 mA	25°C		0.1		
					–40°C to +85°C		0.1		
					–40°C to +125°C		0.3		
		4.5	V_{Bn} = 3.15 V	I_A = -30 mA	25°C		0.1		
					–40°C to +85°C		0.1		
					–40°C to +125°C		0.2		
$r_{on(flat)}$	ON resistance flatness(2) (4) (6)	1.65	0 ≤ V_{Bn} ≤ V_{CC}	I_A = -4 mA	25°C		110		Ω
					–40°C to +85°C		110		
					–40°C to +125°C		110		
		2.3		I_A = -8 mA	25°C		26		
					–40°C to +85°C		26		
					–40°C to +125°C		40		
		3		I_A = -24 mA	25°C		9		
					–40°C to +85°C		9		
					–40°C to +125°C		10		
		4.5		I_A = -30 mA	25°C		4		
					–40°C to +85°C		4		
					–40°C to +125°C		5		
I_{off} (7)	Switch OFF leakage current	1.65 to 5.5	0 ≤ V_I , V_O ≤ V_{CC}		25°C		±0.05	±0.1	μA
					–40°C to +85°C			±1	
					–40°C to +125°C			±1	
$I_{S(on)}$	ON-state switch leakage current	5.5	V_I = V_{CC} or GND, V_O = Open		25°C			±0.1	μA
					–40°C to +85°C			±1	
					–40°C to +125°C			±1	
I_{IN}	Control input current	0 to 5.5	0 ≤ V_{IN} ≤ V_{CC}		25°C		±0.05	±0.1	μA
					–40°C to +85°C			±1	
					–40°C to +125°C			±1	

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Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{CC}	Supply current	5.5	S = V_{CC} or GND	25°C			1	µA
				–40°C to +85°C			10	
				–40°C to +125°C			35	
ΔI_{CC}	Quiescent Device Current, I_{DD} Max	5.5	S = V_{CC} - 0.6 V	25°C			500	µA
				–40°C to +85°C			500	
				–40°C to +125°C			500	
C_I	Control input capacitance	5	S (VDD/2)	25°C		2.7		pF
				–40°C to +85°C		2.7		
				–40°C to +125°C		2.7		
$C_{io(off)}$	Switch input/output capacitance	5	Bn (VDD/2)	25°C		5.2		pF
				–40°C to +85°C		5.2		
				–40°C to +125°C		5.2		
$C_{io(on)}$	Switch input/output capacitance	5	Bn (VDD/2)	25°C		17.3		pF
				–40°C to +85°C		17.3		
				–40°C to +125°C		17.3		
			A (VDD/2)	25°C		17.3		
				–40°C to +85°C		17.3		
				–40°C to +125°C		17.3		

(1) T_A = 25C
(2) Measured by the voltage drop between I/O pins at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages on the two (A or B) ports.
(3) Specified by design
(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$ measured at identical V_{CC}, temperature, and voltage levels
(5) This parameter is characterized, but not production tested.
(6) Flatness is defined as the difference between the maximum and minimum values of on-state resistance over the specified range of conditions.
(7) I_{off} is the same as $I_{S(off)}$ (off-state switch leakage current).

5.6 Switching Characteristics 85C (DBV, DCK)

T_A = -40 to +85°C

Parameter		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	NOM	MAX	UNIT
t_{pd}	R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}	A or Bn	Bn or A	1.8 V ± 0.15 V			2	ns
				2.5 V ± 0.2 V			1.2	
				3.3 V ± 0.3 V			0.8	
				5 V ± 0.5 V			0.3	
t_{en}	R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}	S	Bn	1.8 V ± 0.15 V	5		24	ns
				2.5 V ± 0.2 V	3.5		14	
				3.3 V ± 0.3 V	2.5		7.6	
				5 V ± 0.5 V	1.7		5.7	
t_{dis}	R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}, $V_▲$ = 0.3V			1.8 V ± 0.15 V	3		13	
				2.5 V ± 0.2 V	2		7.5	
				3.3 V ± 0.3 V	1.5		6	
				5 V ± 0.5 V	0.8		5	

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T_A = -40 to +85℃

Parameter		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	NOM	MAX	UNIT
T_{B-M}	Break before make time			1.8 V ± 0.15 V	0.5			ns
				2.5 V ± 0.2 V	0.5			
				3.3 V ± 0.3 V	0.5			
				5 V ± 0.5 V	0.5			

5.7 Switching Characteristics 125C (DBV, DCK)

T_A = -40 to +125℃

Parameter		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	NOM	MAX	UNIT
t_{pd}	R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}	A or Bn	Bn or A	1.8 V ± 0.15 V			2	ns
				2.5 V ± 0.2 V			1.2	
				3.3 V ± 0.3 V			0.8	
				5 V ± 0.5 V			0.5	
t_{en}	R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}	S	Bn	1.8 V ± 0.15 V	1		24.5	ns
				2.5 V ± 0.2 V	1		14.5	
				3.3 V ± 0.3 V	2.5		8	
				5 V ± 0.5 V	1.7		7	
t_{dis}	R_L = 250Ω, C_L = 50pF, V_{load} = V_{CC}, $V_▲$ = 0.3V			1.8 V ± 0.15 V	2.5		13.5	
				2.5 V ± 0.2 V	2		8	
				3.3 V ± 0.3 V	1.5		6.5	
				5 V ± 0.5 V	0.8		5	
T_{B-M}	Break before make time			1.8 V ± 0.15 V	0.5			ns
				2.5 V ± 0.2 V	0.5			
				3.3 V ± 0.3 V	0.5			
				5 V ± 0.5 V	0.5			

5.8 Switching Characteristics 85C (YZP, DSF. DTB. DRY, DRL)

T_A = -40 to +85℃

Parameter		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	NOM	MAX	UNIT
t_{pd}	R_L = 500Ω, C_L = 50pF, V_{load} = V_{CC}	A or Bn	Bn or A	1.8 V ± 0.15 V			2	ns
				2.5 V ± 0.2 V			1.2	
				3.3 V ± 0.3 V			0.8	
				5 V ± 0.5 V			0.3	
t_{en}	R_L = 500Ω, C_L = 50pF, V_{load} = V_{CC}	S	Bn	1.8 V ± 0.15 V	7		24	ns
				2.5 V ± 0.2 V	3.5		14	
				3.3 V ± 0.3 V	2.5		7.6	
				5 V ± 0.5 V	1.7		5.7	
t_{dis}	R_L = 500Ω, C_L = 50pF, V_{load} = V_{CC}, $V_Δ$ = 0.3V			1.8 V ± 0.15 V	3		13	
				2.5 V ± 0.2 V	2		7.5	
				3.3 V ± 0.3 V	1.5		5.3	
				5 V ± 0.5 V	0.8		3.8	

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T_A = -40 to +85℃

Parameter		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	NOM	MAX	UNIT
T_{B-M}	Break before make time			1.8 V ± 0.15 V	0.5			ns
				2.5 V ± 0.2 V	0.5			
				3.3 V ± 0.3 V	0.5			
				5 V ± 0.5 V	0.5			

5.9 Switching Characteristics 125C (YZP, DSF. DTB. DRY, DRL)

T_A = -40 to +125℃

Parameter		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	NOM	MAX	UNIT
t_{pd}	R_L = 500Ω, C_L = 50pF, V_{load} = V_{CC}	A or Bn	Bn or A	1.8 V ± 0.15 V			2	ns
				2.5 V ± 0.2 V			1.2	
				3.3 V ± 0.3 V			0.8	
				5 V ± 0.5 V			0.5	
t_{en}	R_L = 500Ω, C_L = 50pF, V_{load} = V_{CC}	S	Bn	1.8 V ± 0.15 V	1		24.5	ns
				2.5 V ± 0.2 V	1		14.5	
				3.3 V ± 0.3 V	2.5		8	
				5 V ± 0.5 V	1.7		6	
t_{dis}	R_L = 500Ω, C_L = 50pF, V_{load} = V_{CC}, V_Δ = 0.3V			1.8 V ± 0.15 V	2.5		13.5	
				2.5 V ± 0.2 V	2		8	
				3.3 V ± 0.3 V	1.5		5.5	
				5 V ± 0.5 V	0.8		4	
T_{B-M}	Break before make time			1.8 V ± 0.15 V	0.5			ns
				2.5 V ± 0.2 V	0.5			
				3.3 V ± 0.3 V	0.5			
				5 V ± 0.5 V	0.5			

5.10 Analog Channel Specifications

over operating free-air temperature range (unless otherwise noted)

Parameter	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	v_{cc}	MIN	NOM	MAX	UNIT
Frequency response (switch on)(1)	A or Bn	Bn or A	R_L = 50 Ω, f_{in} = sine wave	1.65 V		340		MHz
				2.3 V		340		
				3 V		340		
				4.5 V		340		
Crosstalk (between switches)(2)	B1 or B2	B2 or B1	R_L = 50 Ω, $f_{i\,n}$ = 10 MHz (sine wave)	1.65 V		-54		dB
				2.3 V		-54		
				3 V		-54		
				4.5 V		-54		
Feed through attenuation (switch off)(2)	A or Bn	Bn or A	C_L = 5 pF, R_L = 50 Ω, f_{in} = 10 MHz (sine wave)	1.65 V		-57		dB
				2.3 V		-57		
				3 V		-57		
				4.5 V		-57		
Charge injection	S (Vs = VDD/2)	A	C_L = 0.1 nF, R_L = 1 MΩ	3.3 V		3		pC
				5 V		7		

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over operating free-air temperature range (unless otherwise noted)

Parameter	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	v_{cc}	MIN	NOM	MAX	UNIT
Total harmonic distortion (YZP, DSF. DTB. DRY, DRL)	A or Bn	Bn or A	V_I = 1.4 V_{p-p}, Vbias = Vcc/2, R_L = 10kΩ, f_{in} = 600 Hz to 20kHz (sine wave)	1.65 V		0.1		%
Total harmonic distortion (DBV, DCK)	A or Bn	Bn or A	V_I = 1.4 V_{p-p}, Vbias = Vcc/2, R_L = 10kΩ, f_{in} = 600 Hz to 20kHz (sine wave)	1.65 V		0.5		%
Total harmonic distortion	A or Bn	Bn or A	V_I = 2.0 V_{p-p}, Vbias = Vcc/2, R_L = 10kΩ, f_{in} = 600 Hz to 20kHz (sine wave)	2.3 V		0.025		%
				3 V		0.015		
				4.5 V		0.01		

(1) Set fin to 0 dBm and provide a bias of 0.4 V. Increase fin frequency until the gain is 3 dB below the insertion loss.
(2) Set fin to 0 dBm and provide a bias of 0.4 V.

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6 Parameter Measurement Information

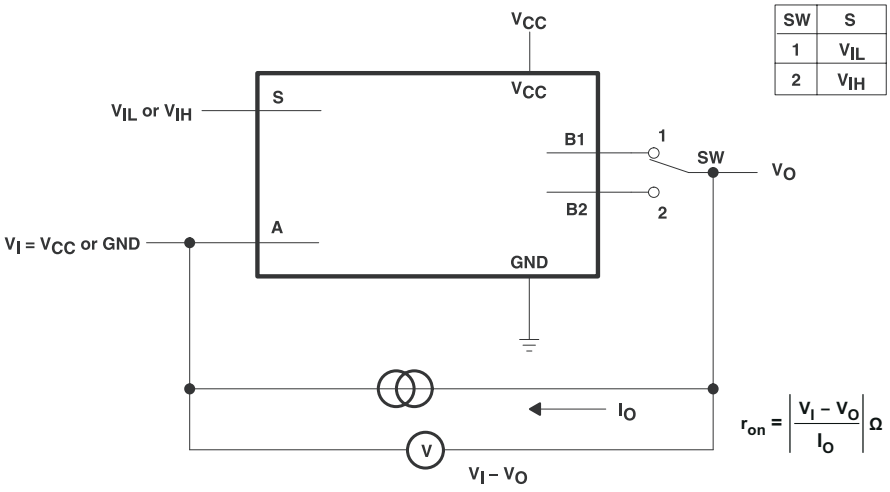
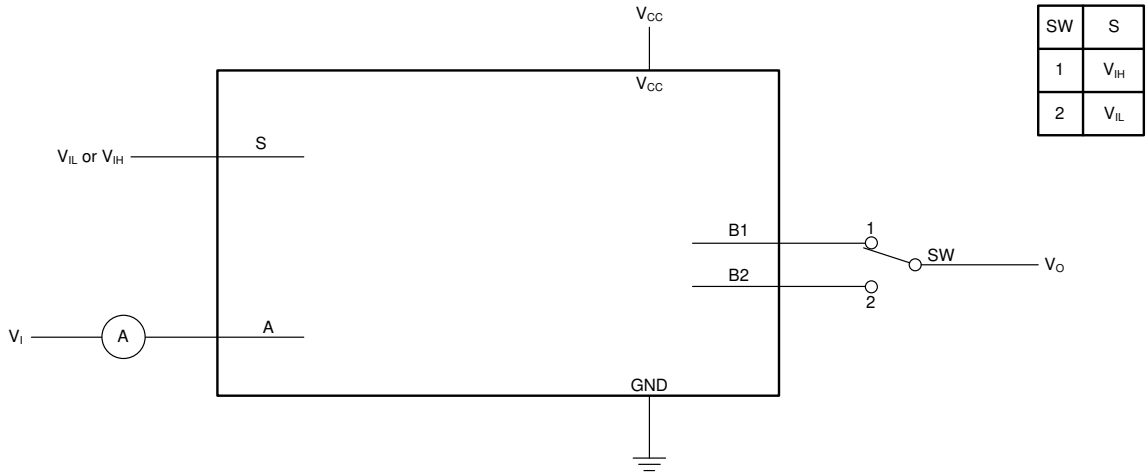


Figure 6-1. ON-State Resistance Test Circuit



Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 6-2. OFF-State Switch Leakage-Current Test Circuit

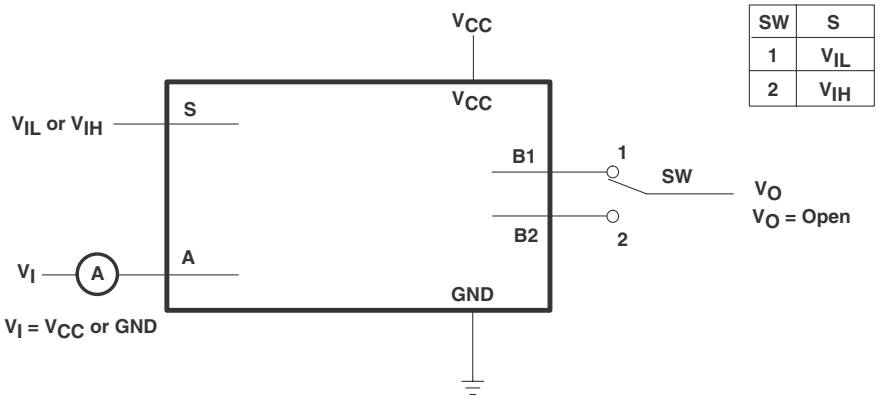
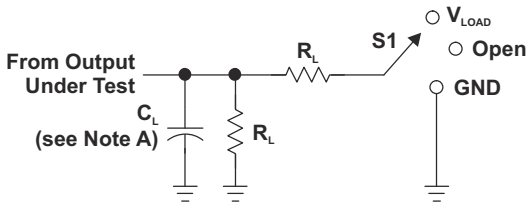


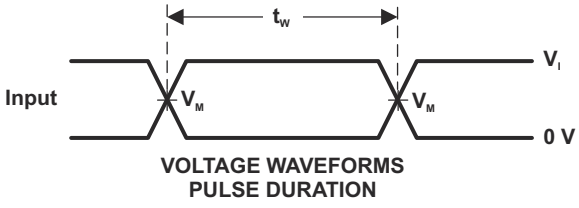
Figure 6-3. ON-State Switch Leakage-Current Test Circuit



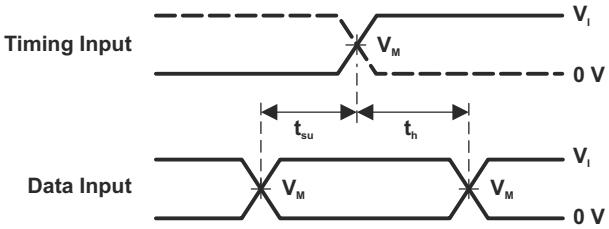
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

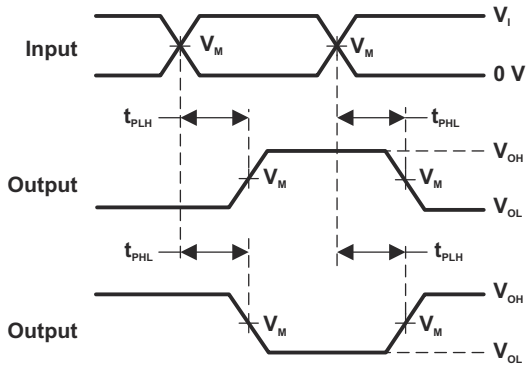
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



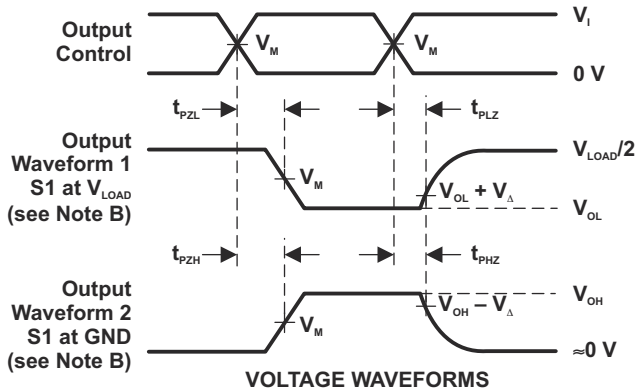
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 6-4. Load Circuit and Voltage Waveforms

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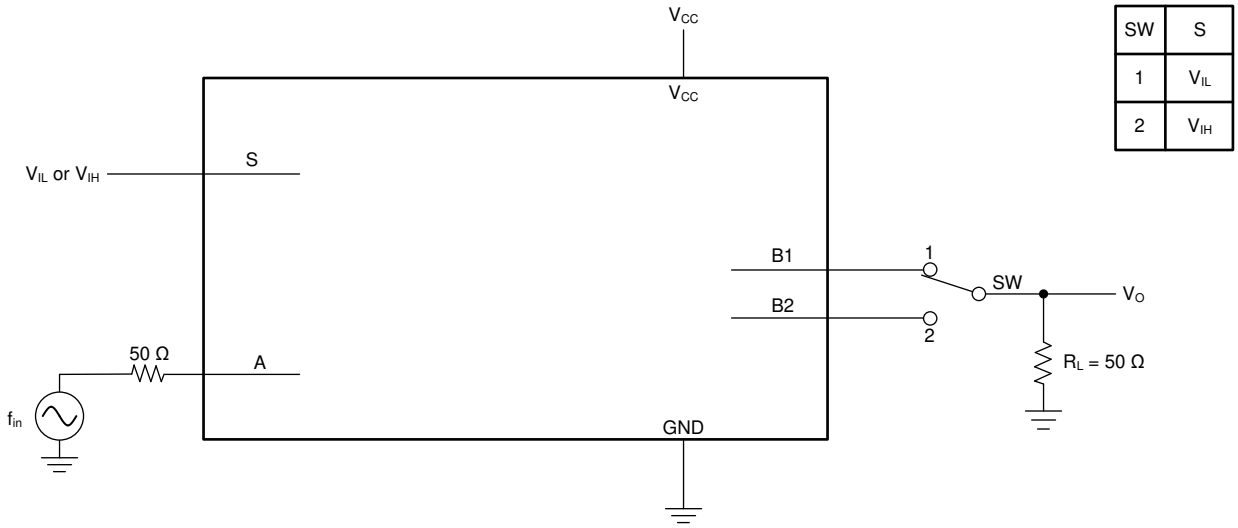

Figure 6-5. Frequency Response (Switch On)

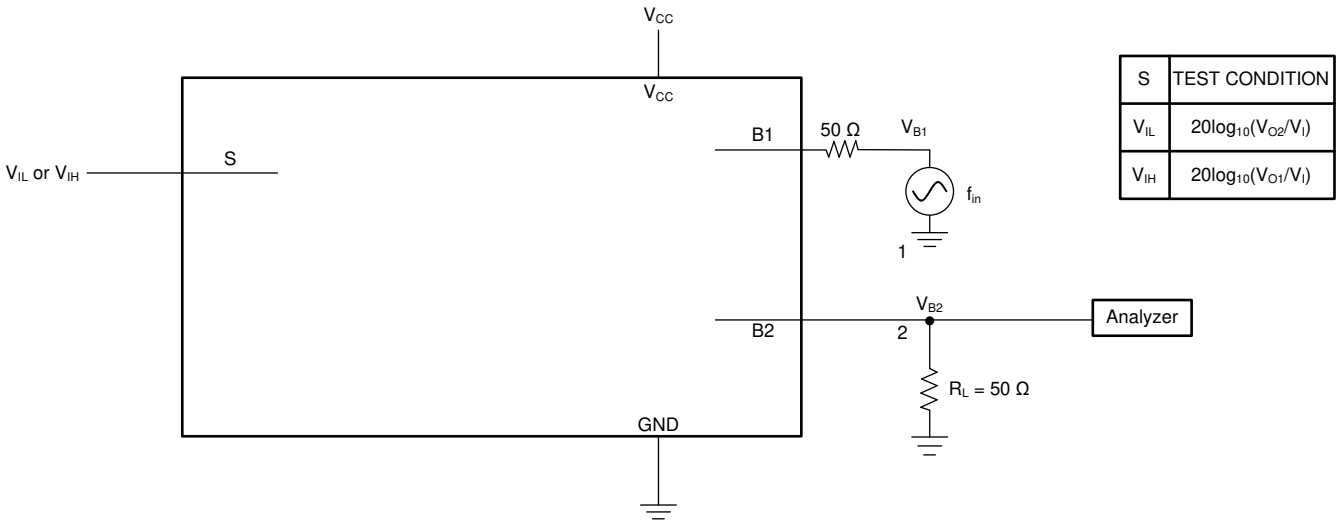

Figure 6-6. Crosstalk (Between Switches)

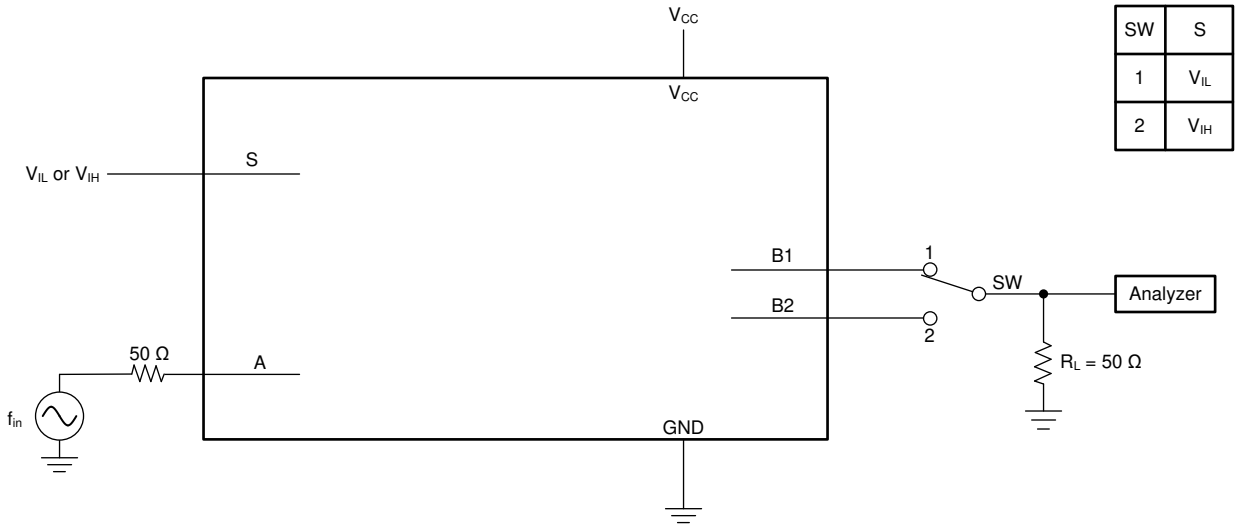

Figure 6-7. Feed Through

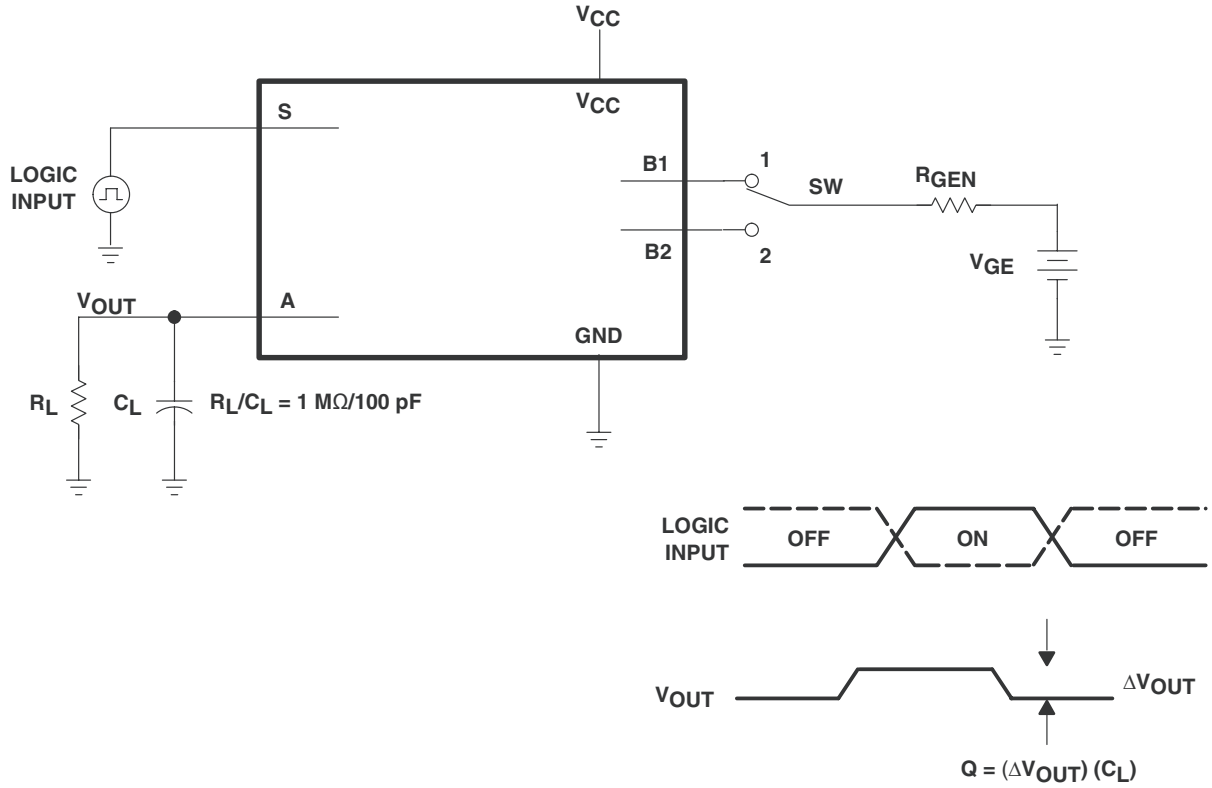

Figure 6-8. Charge-Injection Test

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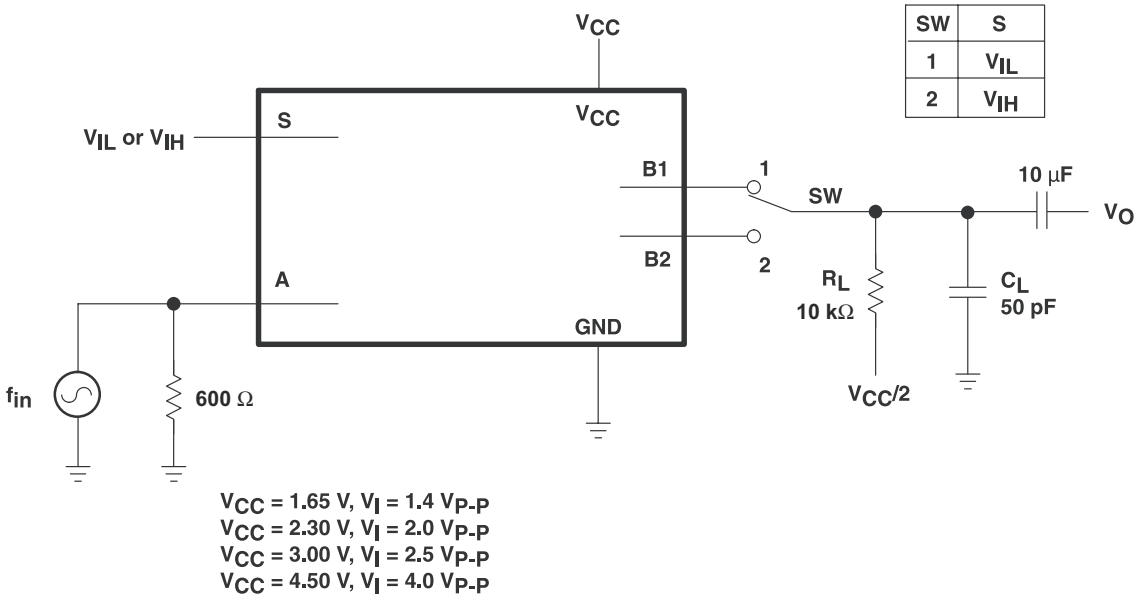

Figure 6-9. Total Harmonic Distortion

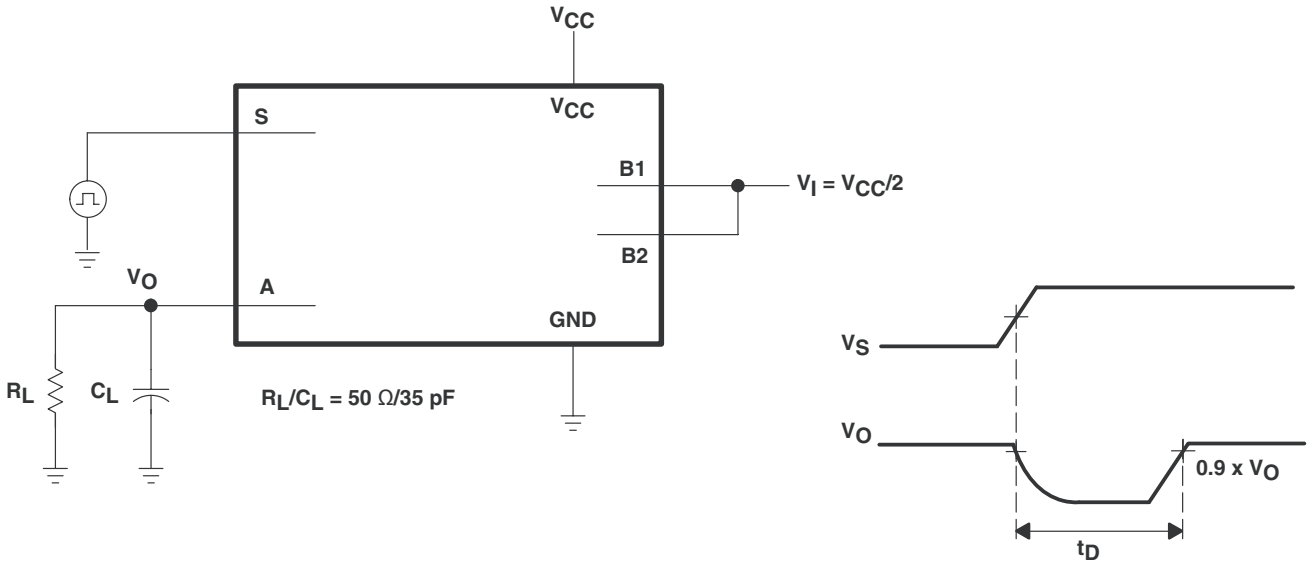

Figure 6-10. Break-Before-Make Internal Timing

7 Detailed Description

7.1 Overview

The SN74LVC1G3157 device is a single-pole double-throw (SPDT) analog switch designed for 1.65V to 5.5V V_{CC} operation. The SN74LVC1G3157 device can handle analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

7.2 Functional Block Diagram

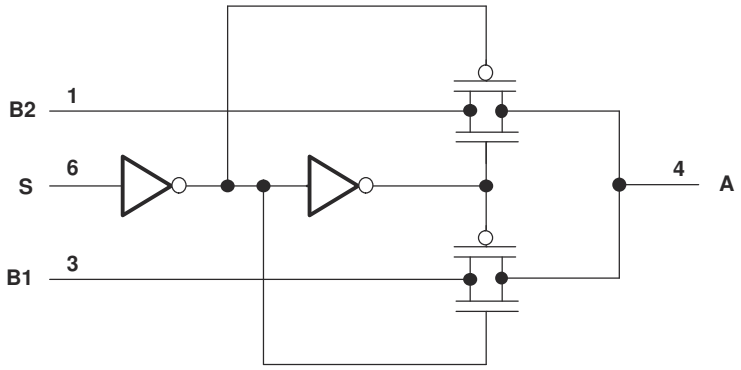

Figure 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

The 1.65V to 5.5V supply operation allows the device to function in many different systems comprised of different logic levels, allowing rail-to-rail signal switching. Either the B1 channel or the B2 channel is activated depending upon the control input. If the control input is low, B1 channel is selected. If the control input is high, B2 channel is selected.

7.4 Device Functional Modes

Table 7-1 lists the ON channel when one of the control inputs is selected.

Table 7-1. Function Table

CONTROL INPUTS	ON CHANNEL
L	B1
H	B2

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74LVC1G3157 SPDT analog switch is flexible enough for use in a variety of circuits such as analog audio routing, power-up monitor, memory sharing, and so on. For details on the applications, see SN74LVC1G3157 and SN74LVC2G53 SPDT Analog Switches.

8.2 Typical Application

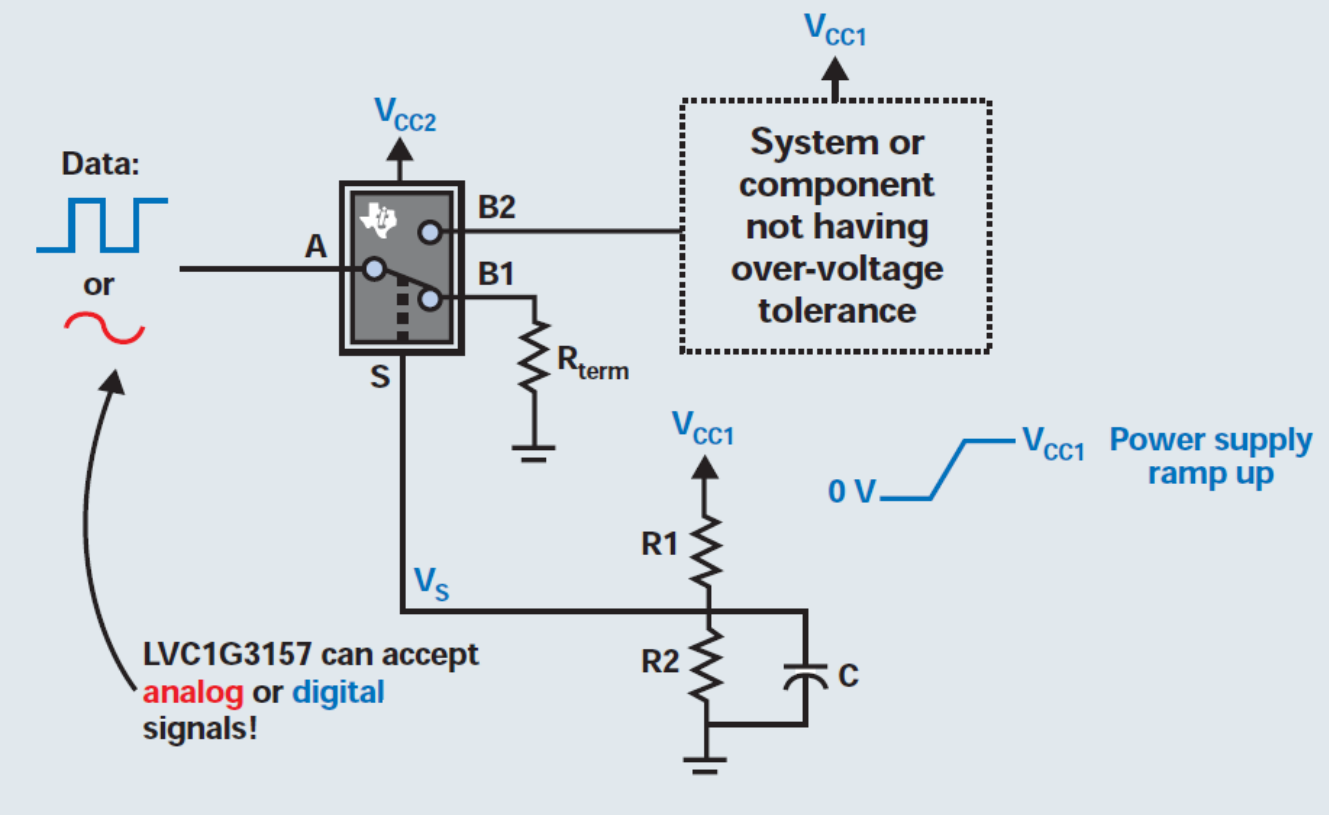

Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

The inputs can be analog or digital, but TI recommends waiting until V_{CC} has ramped to a level in *Section 5.4* before applying any signals. Appropriate termination resistors should be used depending on the type of signal and specification. The Select pin should not be left floating; either pull up or pull down with a resistor that can be overdriven by a GPIO.

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8.2.2 Detailed Design Procedure

Using this circuit idea, a system designer can ensure a component or subsystem power has ramped up before allowing signals to be applied to its input. This is useful for integrated circuits that do not have overvoltage tolerant inputs. The basic idea uses a resistor divider on the VCC1 power rail, which is ramping up. The RC time constant of the resistor divider further delays the voltage ramp on the select pin of the SPDT bus switch. By carefully selecting values for R1, R2, and C, it is possible to ensure that VCC1 will reach its nominal value before the path from A to B2 is established, thus preventing a signal being present on an I/O before the device/system is powered up. To ensure the minimum desired delay is achieved, the designer should use Equation 1 to calculate the time required from a transition from ground (0V) to half the supply voltage (VCC1/2).

$$\text{Set}\left(\frac{R2}{R1 + R2} \times V_{CC1} > V_{IH}\right) \text{of the select pin} \tag{1}$$

Choose Rs and C to achieve the desired delay. When V_S goes high, the signal will be passed.

8.2.3 Application Curve

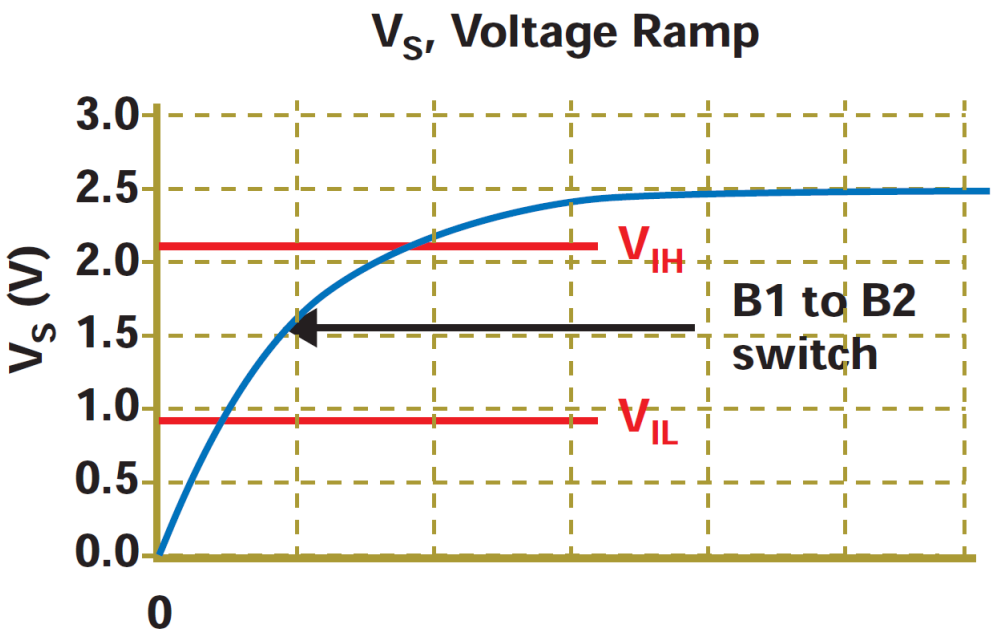

Figure 8-2. V_S Voltage Ramp

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9 Power Supply Recommendations

Most systems have a common 3.3V or 5V rail that can supply the V_{CC} pin of this device. If this is not available, a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) can be used to provide supply to this device from another voltage rail.

10 Layout

10.1 Layout Guidelines

TI recommends keeping signal lines as short as possible. TI also recommends incorporating microstrip or stripline techniques when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50Ω or 75Ω, as required by the application. Do not place this device too close to high-voltage switching components, as they may interfere with the device.

10.2 Layout Example

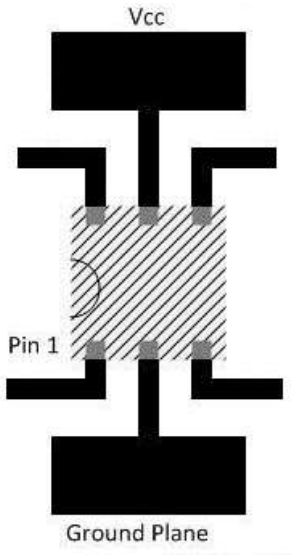

Figure 10-1. Recommended Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*
- Texas Instruments, *SN74LVC1G3157 and SN74LVC2G53 SPDT Analog Switches*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (May 2025) to Revision O (June 2025)	Page
• Separated relevant DBV and DCK specifications from other packages	5

Changes from Revision M (August 2022) to Revision N (May 2025)	Page
• ABS max supply voltage changed	5
• Updated thermal parameters for DBV and DCK	6
• r_{range} updated	7
• Updated enable timing for 85C 1.8V and 125C 5V conditions	9
• Updated disable timing for 85C 5V and 125C 3.3V, 5V conditions	9
• Updated THD test conditions and 1.65V specification	11

Changes from Revision L (May 2017) to Revision M (August 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

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- Updated the *Pin Configuration and Functions* section.....3
- Updated the equation in the *Detailed Design Procedure* section.....20

Changes from Revision K (January 2017) to Revision L (May 2017) **Page**

- Deleted *Feature* "Useful for Both Analog and Digital Applications" 1
- Deleted *Feature* "High Degree of Linearity" 1
- Changed the first sentence of the *Description* From: "This single-pole double-throw (SPDT)..." To: "This single channel single pole double-throw (SPDT)..." 1
- Added the X2SON (DTB) package to the *Device Information* 1
- Added the X2SON (DTB) Package, to the *Pin Configuration and Functions* 3
- Changed Figure 6-2, From: SW1 = V_{IL} to SW1 = V_{IH}, From: SW2 = V_{IH} to: SW2 = V_{IL} 13
- Changed Figure 6-5 13
- Added a series 50-Ω resistor on B1 in Figure 6-6 13
- Changed Figure 6-7 13

Changes from Revision J (June 2016) to Revision K (January 2017) **Page**

- Added new applications to *Applications* section 1

Changes from Revision I (June 2015) to Revision J (June 2016) **Page**

- Deleted 200V Machine Model (A115-A) from *Features* 1
- Changed *Feature* From: "Operating Frequency Typically 300MHz at Room Temperature" To: "Operating Frequency Typically 340MHz at Room Temperature".....1
- Updated *Device Information* table.....1
- Updated pinout images for all Packages.....3
- Added *Receiving Notification of Documentation Updates* section.....22

Changes from Revision H (May 2012) to Revision I (June 2015) **Page**

- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Updated *Features*.....1

Changes from Revision G (September 2011) to Revision H (May 2012) **Page**

- Changed YZP with correct pin labels. 3

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVC1G3157DBVR1G4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC55
74LVC1G3157DBVR1G4.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC55
74LVC1G3157DBVR1G4.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC55
74LVC1G3157DRLRG4	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C57
74LVC1G3157DRLRG4.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C57
74LVC1G3157DSFRG4	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
74LVC1G3157DSFRG4.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CC55, CC5F, CC5K, CC5R) CC5S
SN74LVC1G3157DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CC55, CC5F, CC5K, CC5R) CC5S
SN74LVC1G3157DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CC55, CC5F, CC5K, CC5R) CC5S
SN74LVC1G3157DCK3	Obsolete	Production	SC70 (DCK) | 6	-	-	Call TI	Call TI	-40 to 125	C5Z
SN74LVC1G3157DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN | NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5R)
SN74LVC1G3157DCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5R)
SN74LVC1G3157DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C55, C5F, C5J, C5R)
SN74LVC1G3157DRLR	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(C57, C5R)
SN74LVC1G3157DRLR.A	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C57, C5R)
SN74LVC1G3157DRLR.B	Active	Production	SOT-5X3 (DRL) | 6	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C57, C5R)
SN74LVC1G3157DRY2	Obsolete	Production	SON (DRY) | 6	-	-	Call TI	Call TI	-40 to 125	C5
SN74LVC1G3157DRYR	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DRYR.A	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DRYR.B	Active	Production	SON (DRY) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DSFR	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG | NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G3157DSFR.A	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DSFR.B	Active	Production	SON (DSF) | 6	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C5
SN74LVC1G3157DTBR	Active	Production	X2SON (DTB) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7X
SN74LVC1G3157DTBR.B	Active	Production	X2SON (DTB) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7X
SN74LVC1G3157YZPR	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C5N
SN74LVC1G3157YZPR.B	Active	Production	DSBGA (YZP) | 6	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C5N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G3157 :

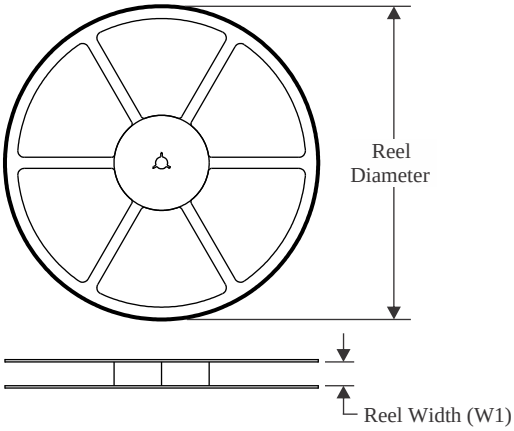
- Automotive : SN74LVC1G3157-Q1

NOTE: Qualified Version Definitions:

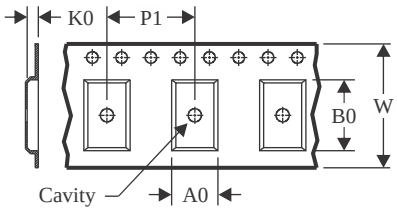
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

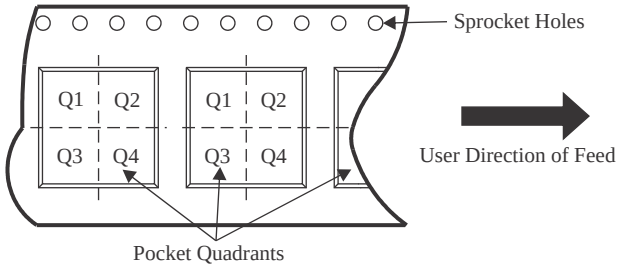


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

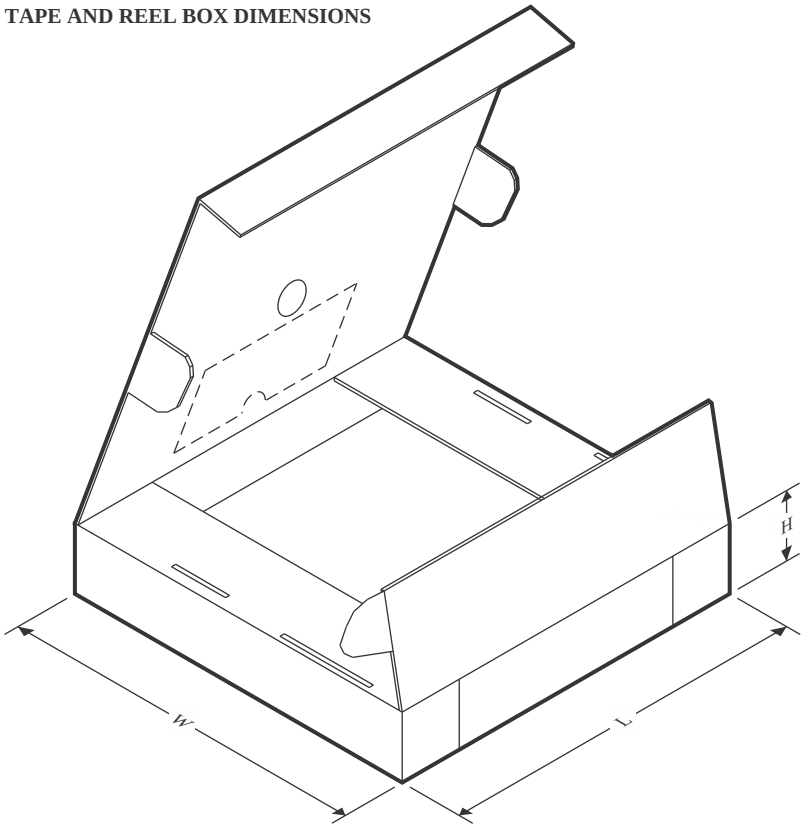
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC1G3157DBVR1G4	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
74LVC1G3157DRLRG4	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
74LVC1G3157DSFRG4	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G3157DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G3157DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74LVC1G3157DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G3157DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G3157DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G3157DTBR	X2SON	DTB	6	3000	180.0	9.5	0.94	1.13	0.41	2.0	8.0	Q2
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

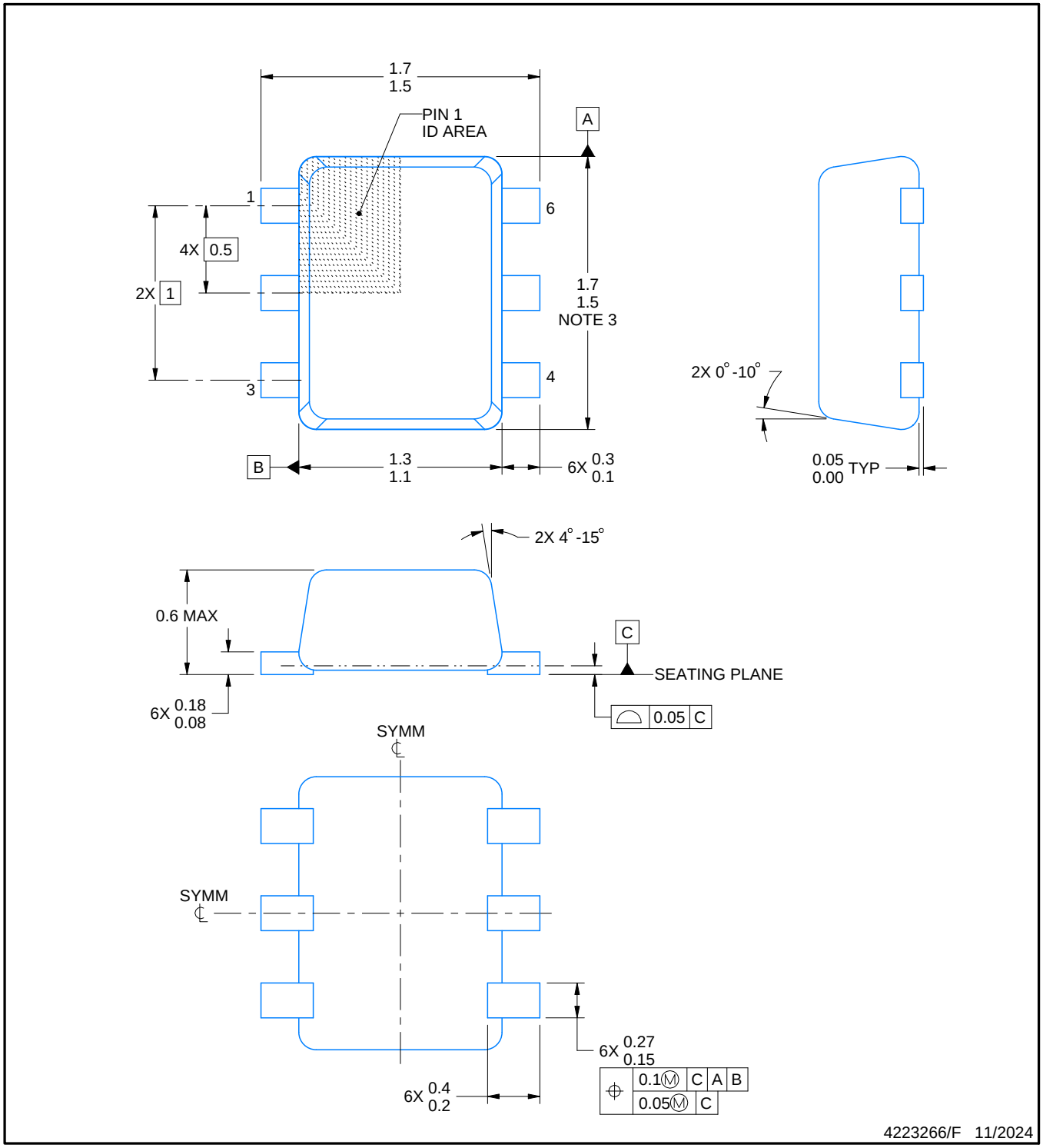
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC1G3157DBVR1G4	SOT-23	DBV	6	3000	210.0	185.0	35.0
74LVC1G3157DRLRG4	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
74LVC1G3157DSFRG4	SON	DSF	6	5000	210.0	185.0	35.0
SN74LVC1G3157DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
SN74LVC1G3157DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC1G3157DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	189.0	185.0	36.0
SN74LVC1G3157DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G3157DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74LVC1G3157DTBR	X2SON	DTB	6	3000	189.0	185.0	36.0
SN74LVC1G3157YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

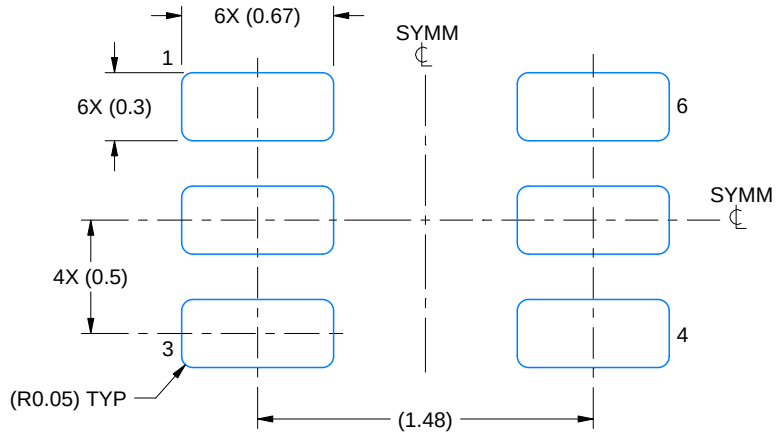
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

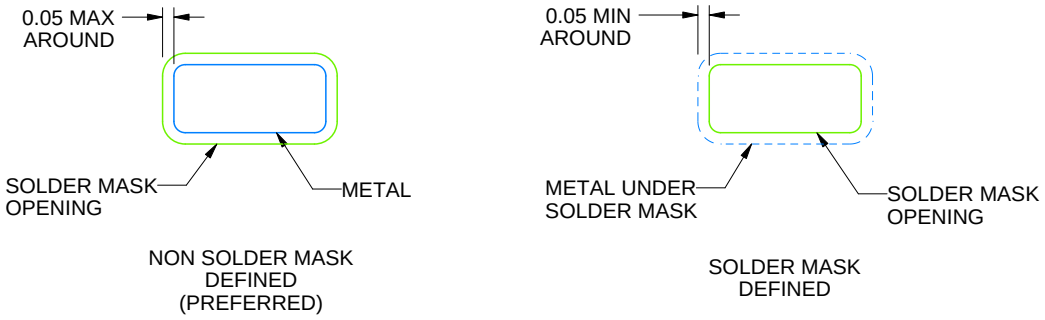
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/F 11/2024

NOTES: (continued)

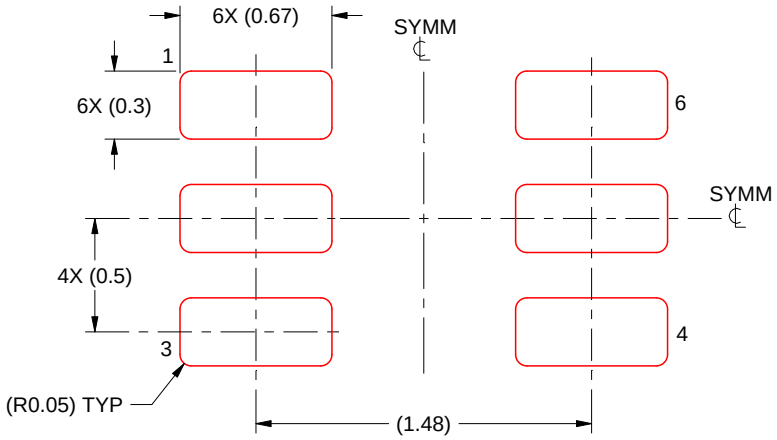
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

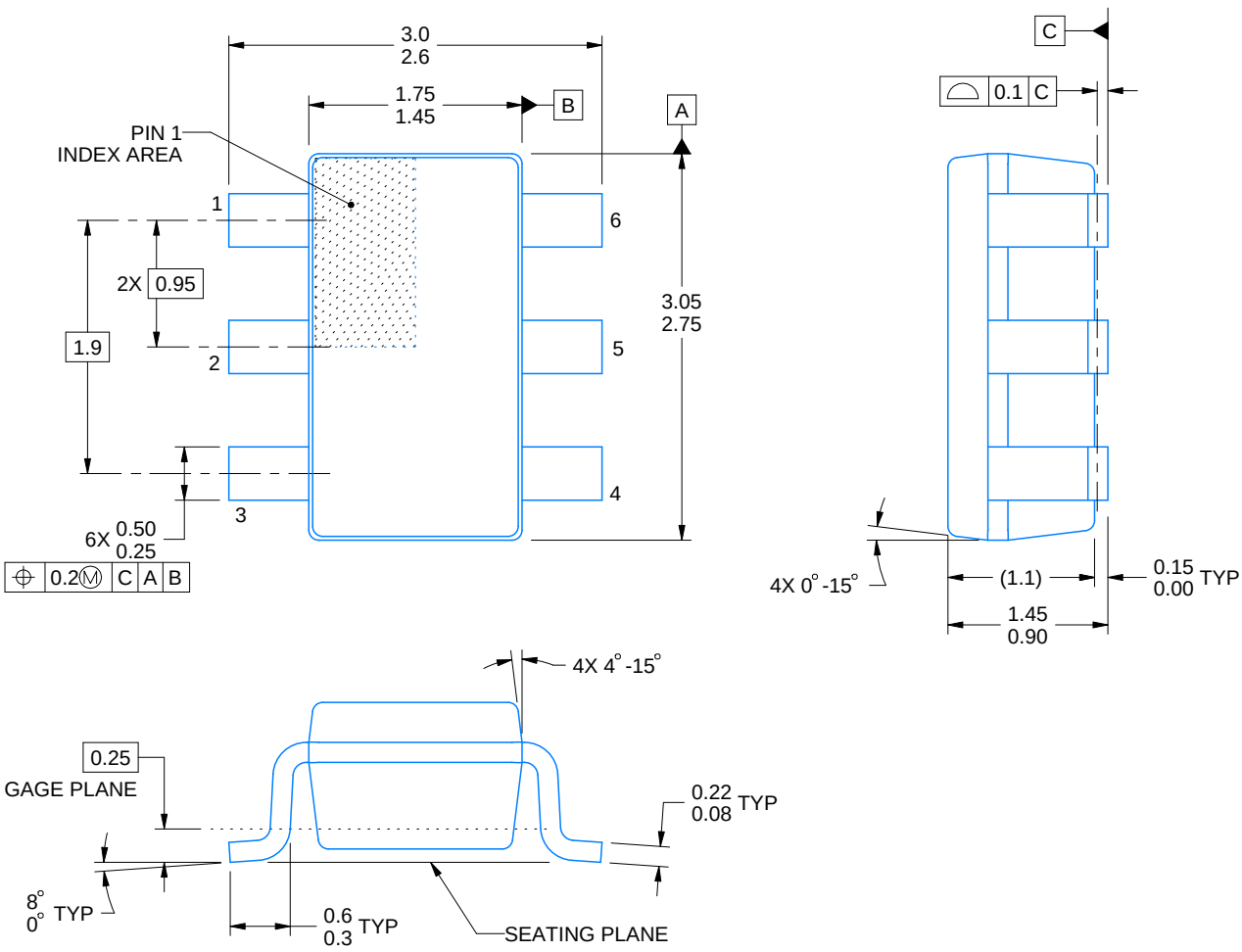
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

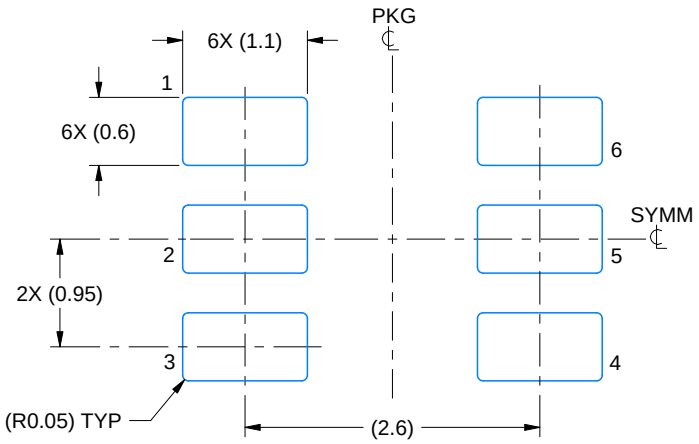
SMALL OUTLINE TRANSISTOR



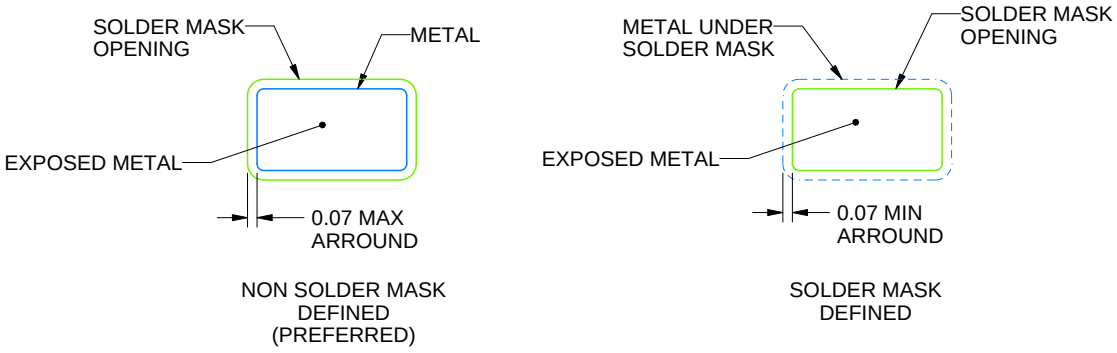
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

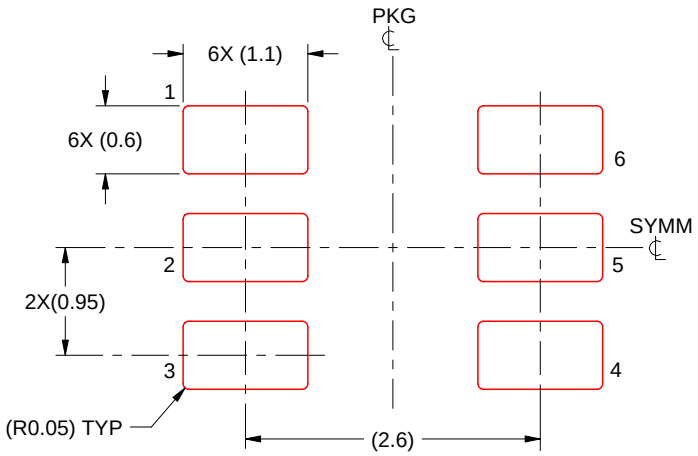


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

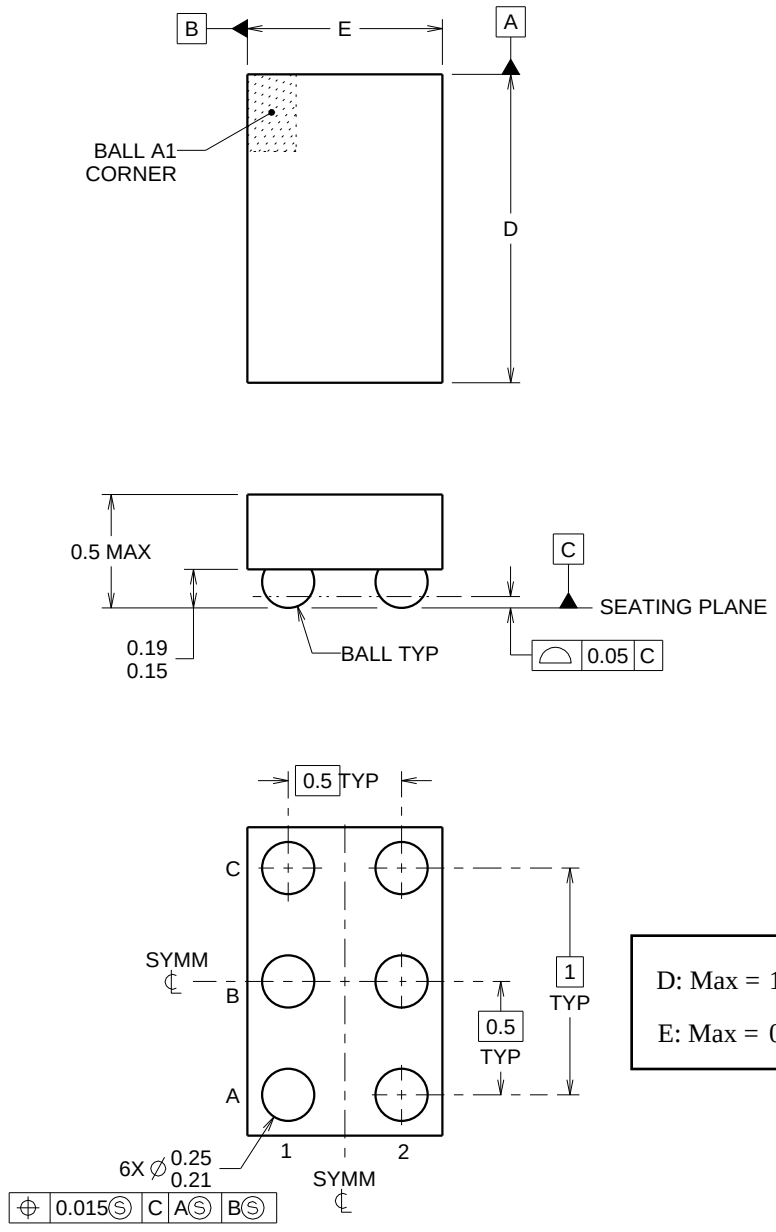
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.418 mm, Min =1.357 mm

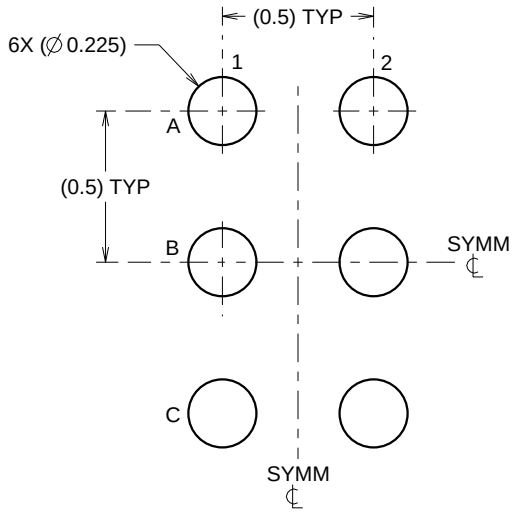
E: Max = 0.918 mm, Min =0.857 mm

4219524/A 06/2014

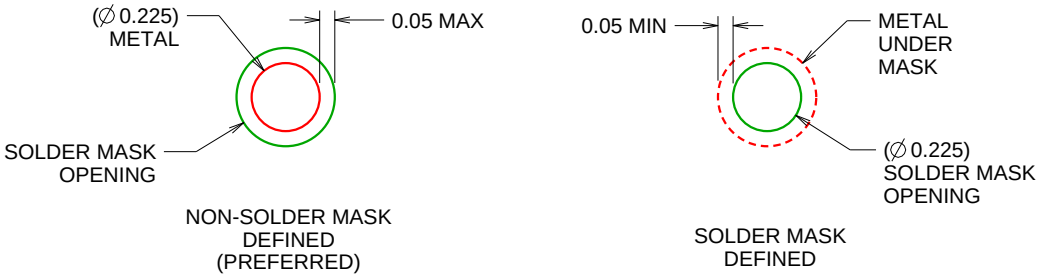
NOTES:

NanoFree Is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

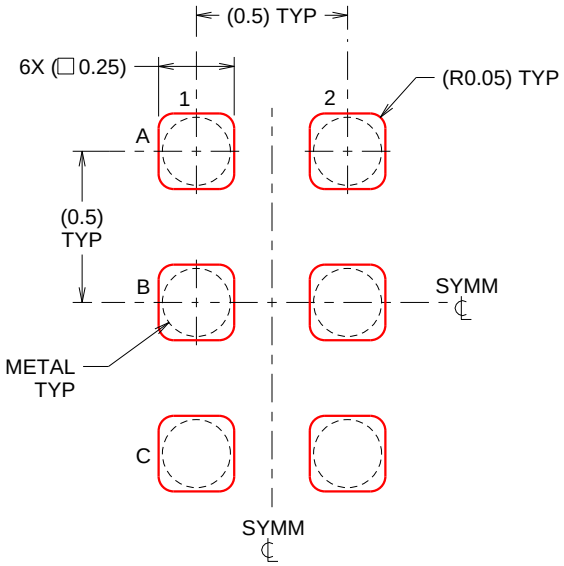
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

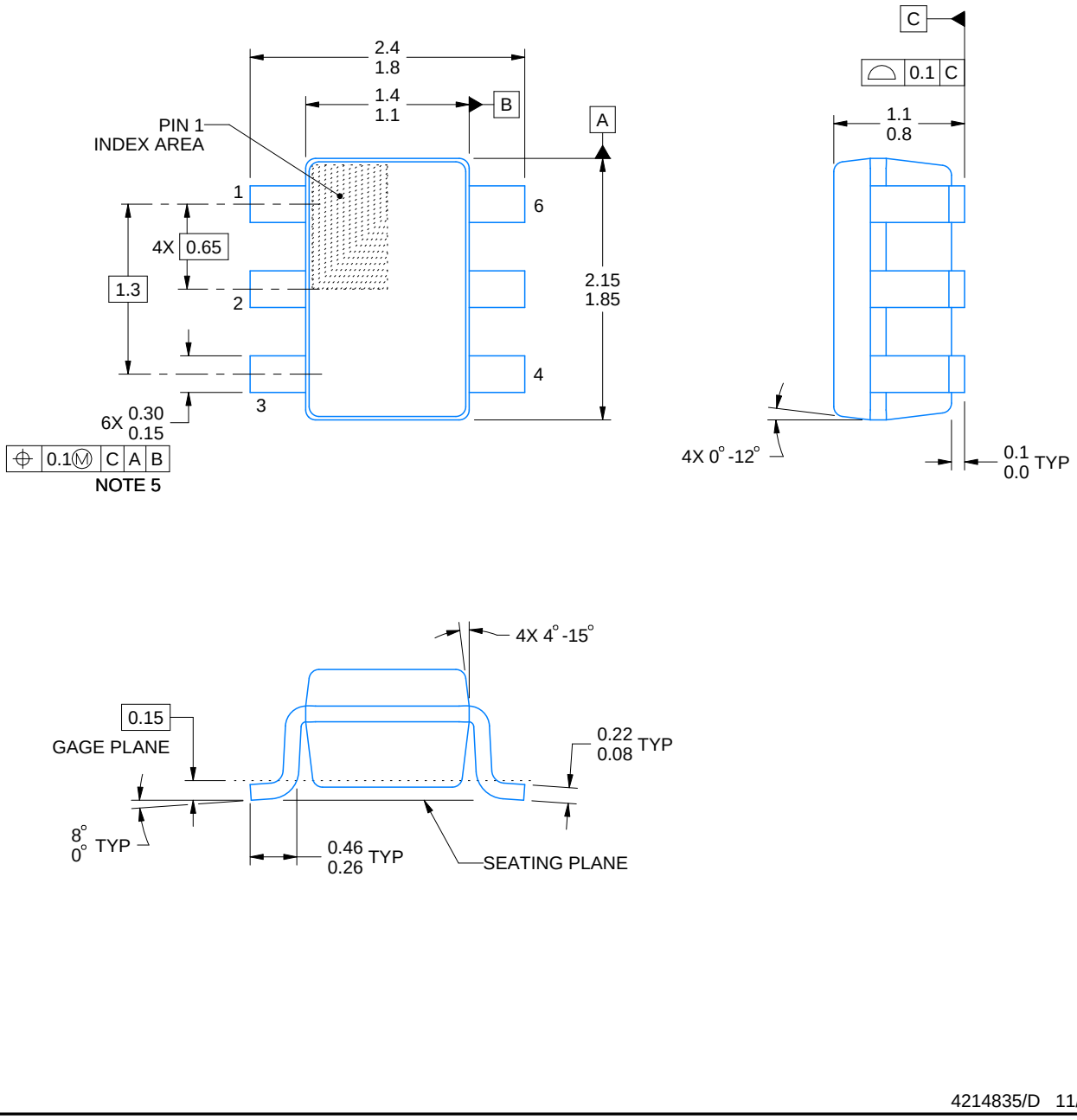
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

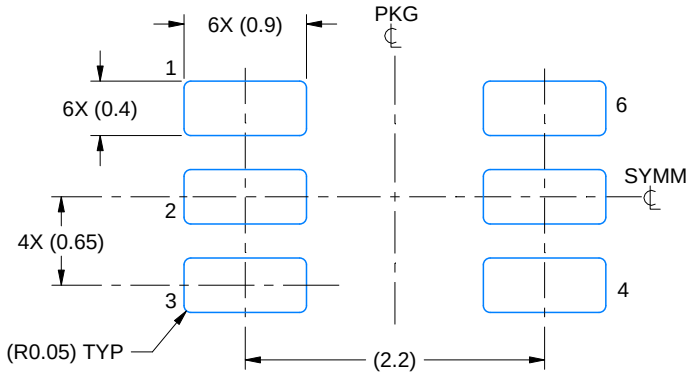
SMALL OUTLINE TRANSISTOR



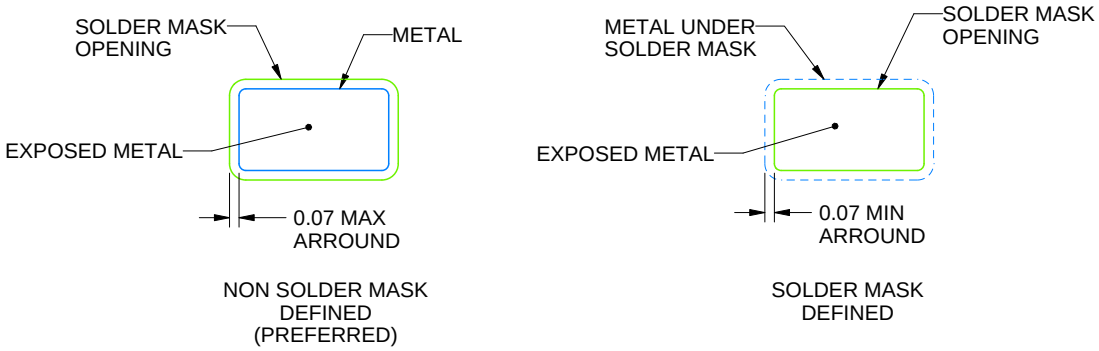
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

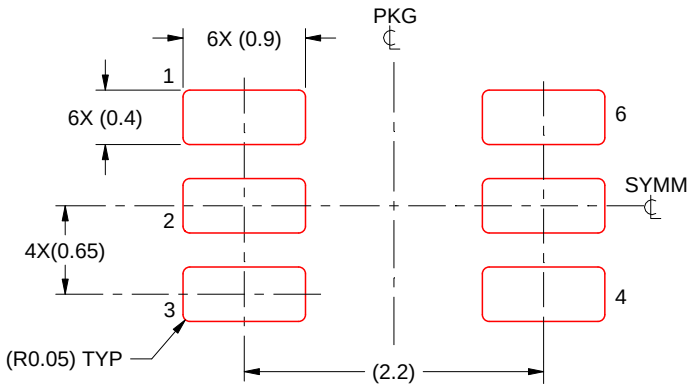


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

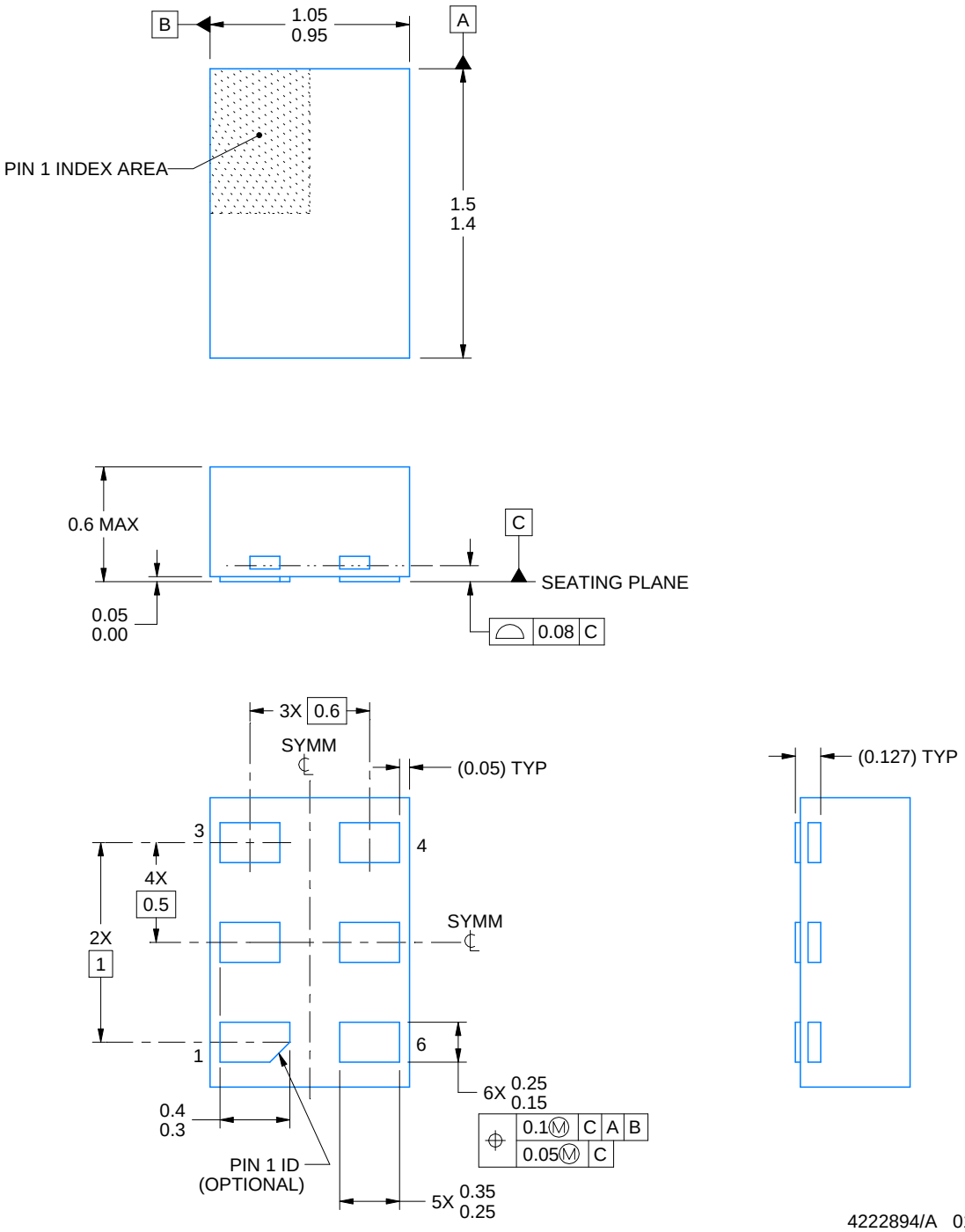
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRY0006A

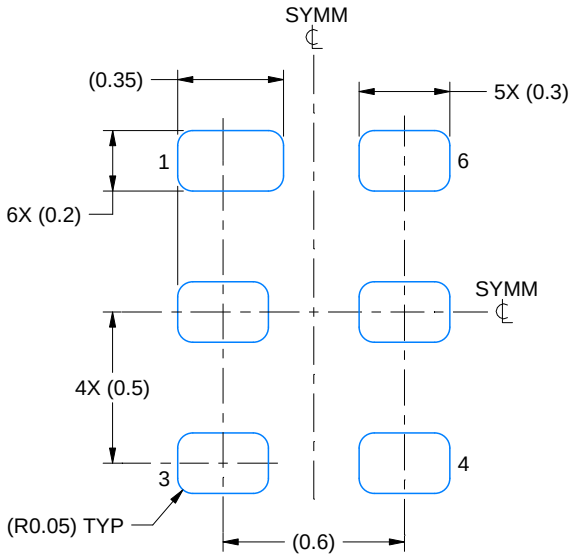
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

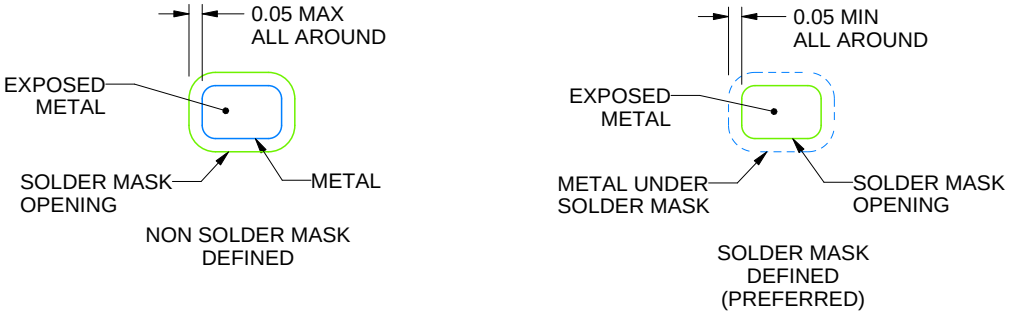


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

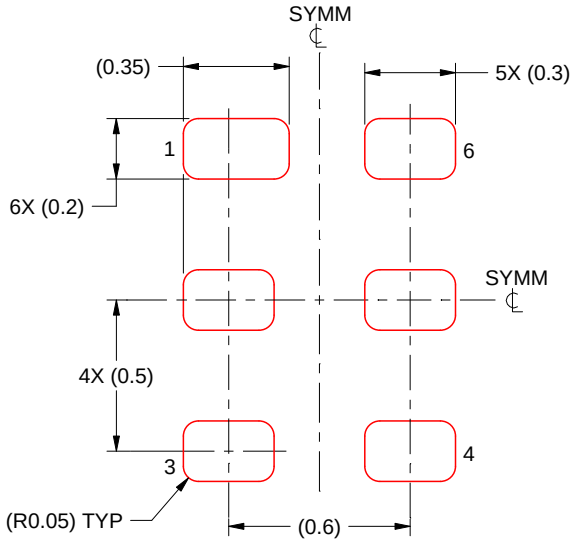
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

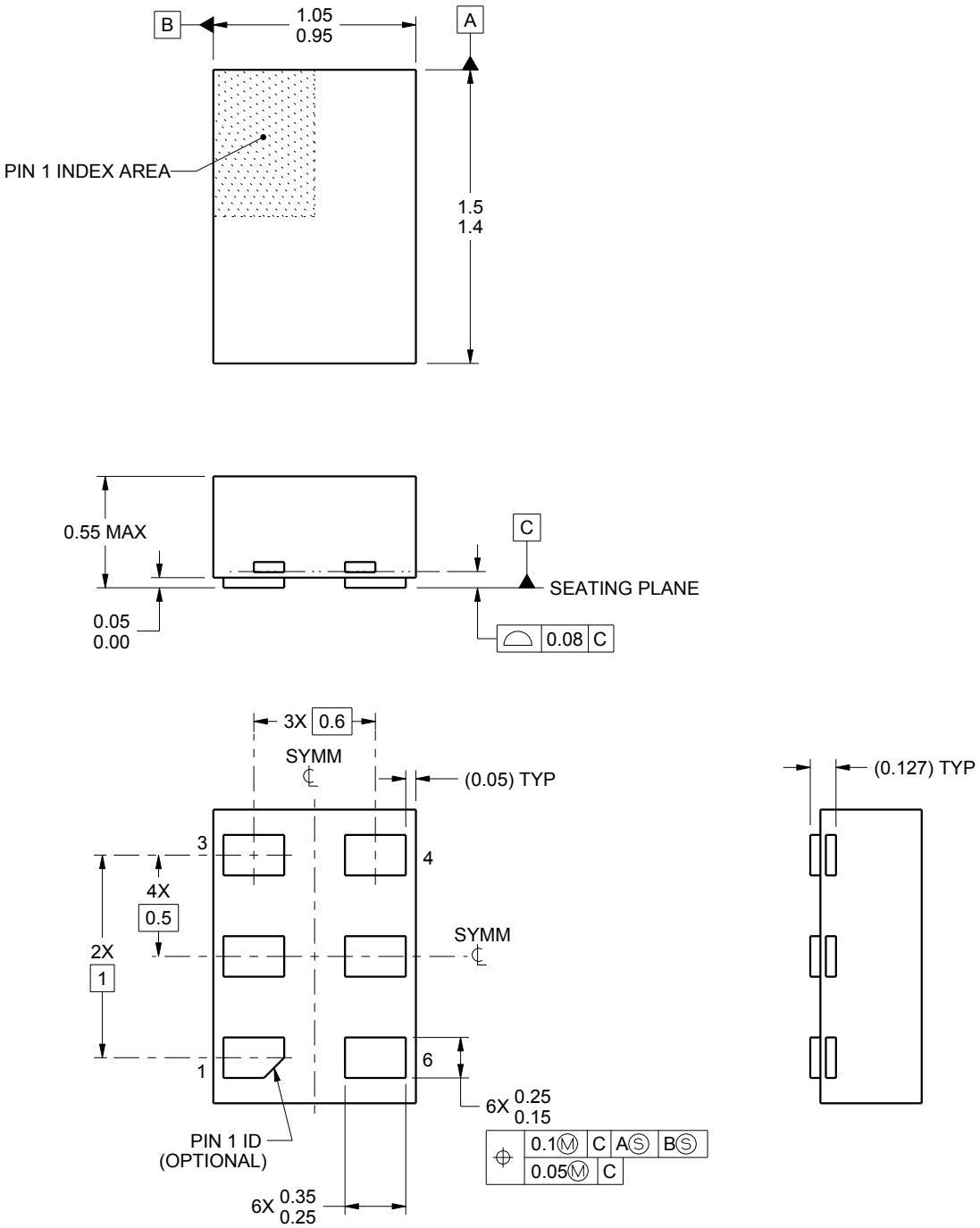
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DRY0006B

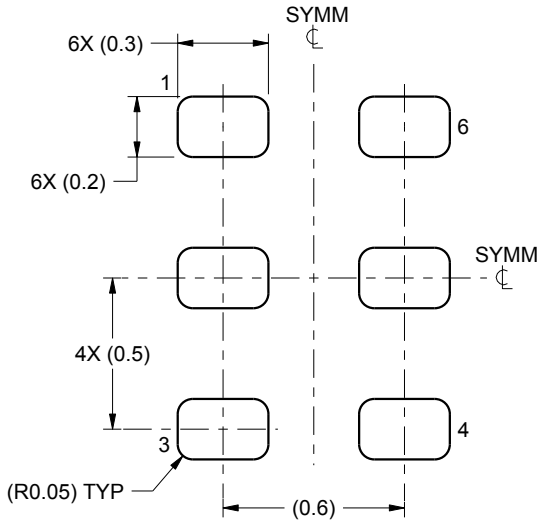
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

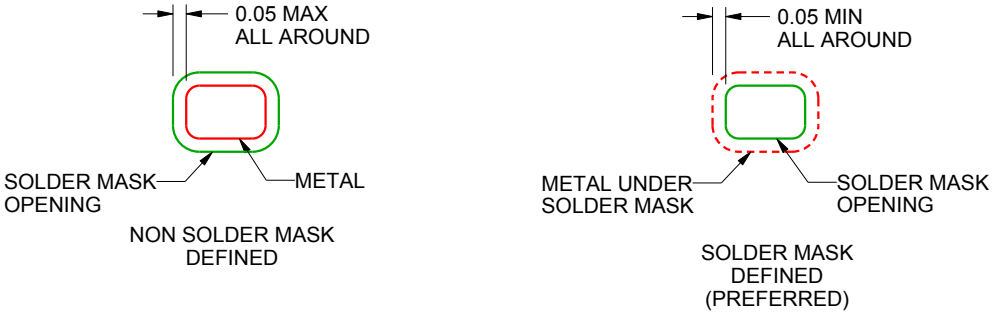


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X

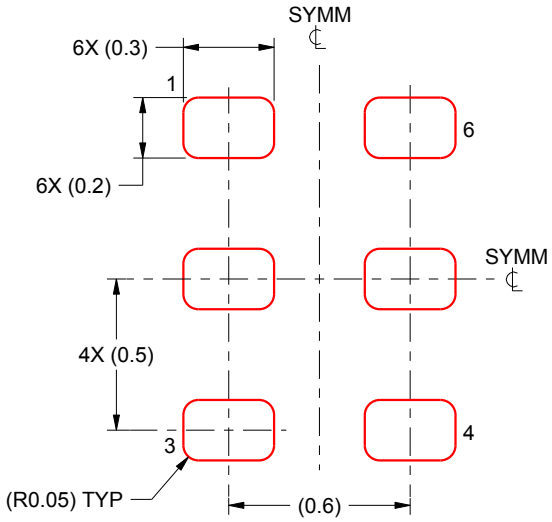


SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

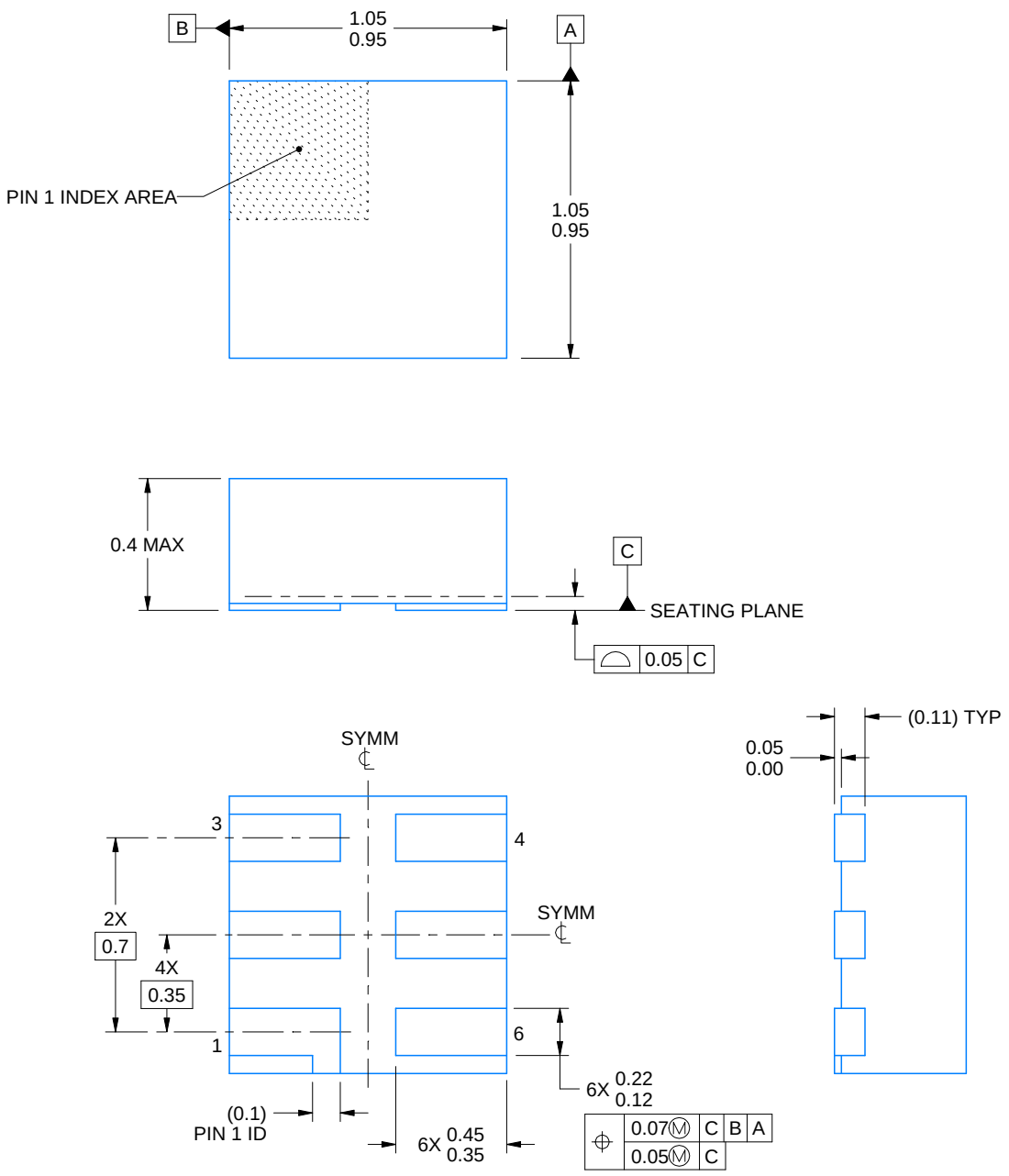
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

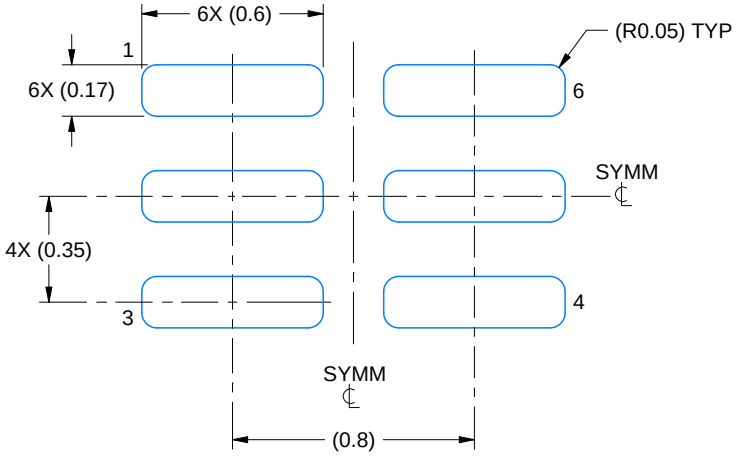
PLASTIC SMALL OUTLINE - NO LEAD



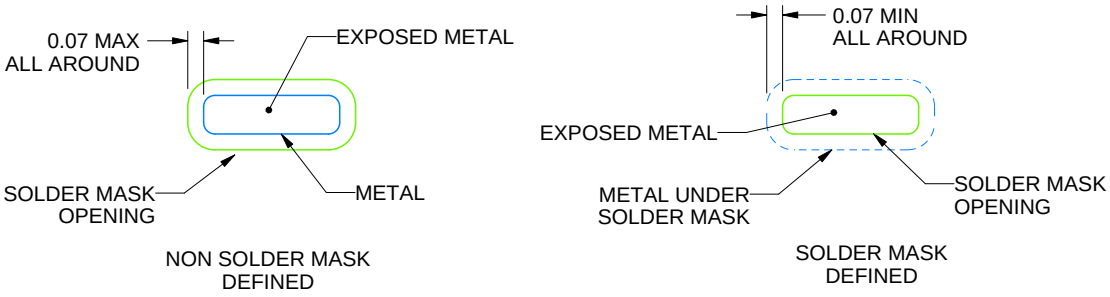
4220597/B 06/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

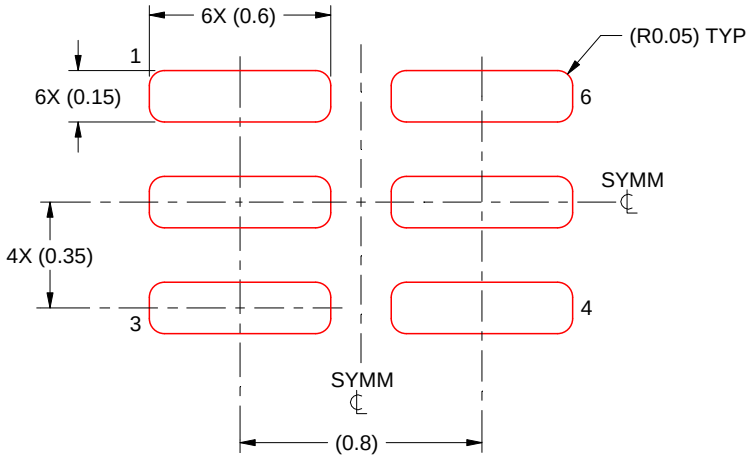
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

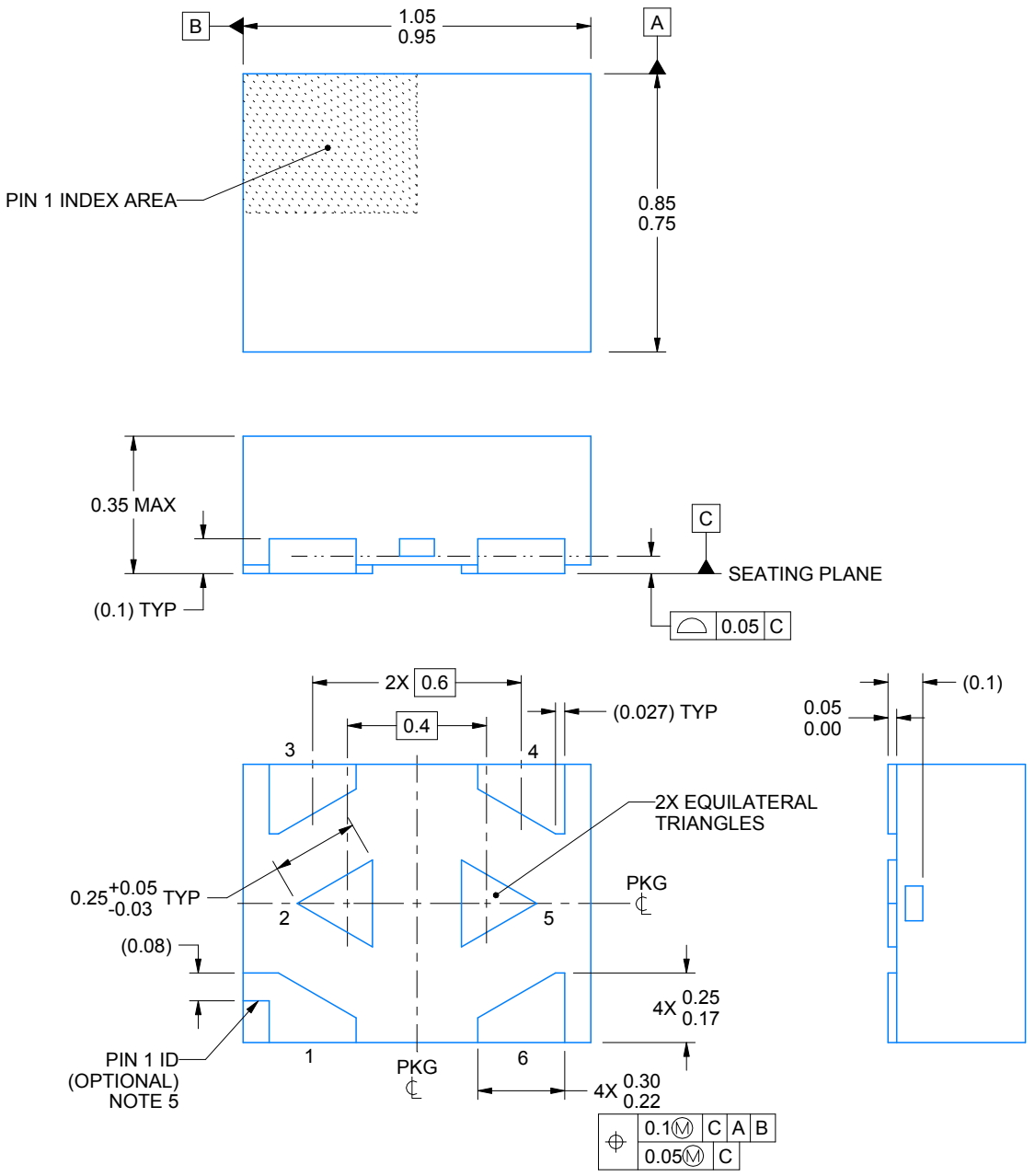
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DTB0006A

PACKAGE OUTLINE

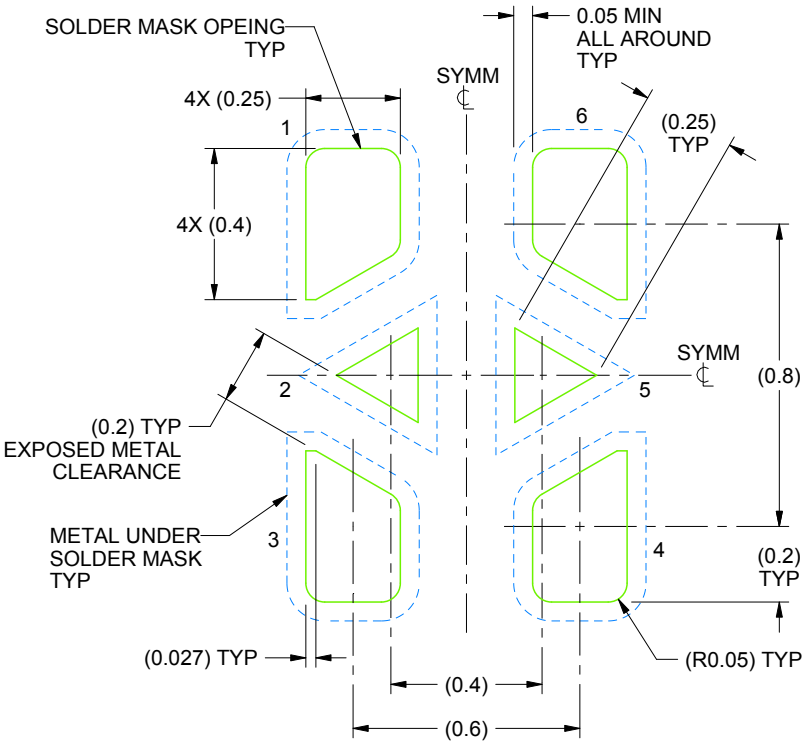
X2SON - 0.35 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

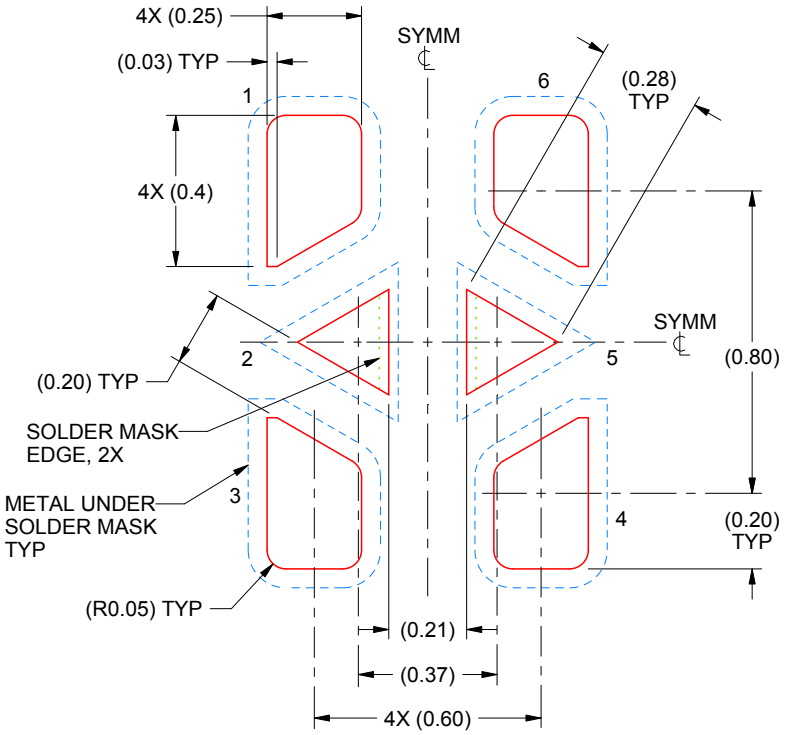


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

4223406/C 02/2019

NOTES: (continued)

6. This package is designed to be soldered to a thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.07 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:50X

4223406/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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