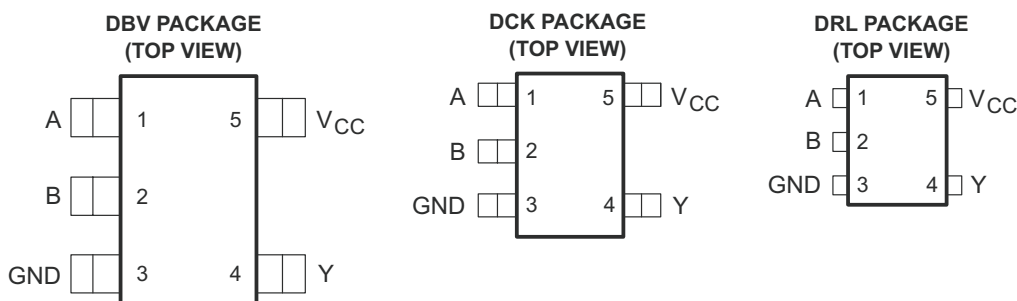


SINGLE 2-INPUT POSITIVE-NAND GATE

Check for Samples: [SN74AHC1G00](#)

FEATURES

- Operating Range 2-V to 5.5-V
- Max t_{pd} of 6.5ns at 5-V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 8 -mA Output Drive at 5-V
- Schmitt Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION

The SN74AHC1G00 performs the Boolean function $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

LOGIC DIAGRAM (POSITIVE LOGIC)


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74AHC1G00

SCLS313N – MARCH 1996 – REVISED MAY 2013

www.ti.com

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		VALUE	UNIT
Supply voltage range, V_{CC}		–0.5 to 7	V
Input voltage range, V_I ⁽²⁾		–0.5 to 7	V
Output voltage range, V_O ⁽²⁾		–0.5 to $V_{CC} + 0.5$	V
Input clamp current, I_{IK} ($V_I < 0$)		–20	mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)		±20	mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±25	mA
Continuous current through V_{CC} or GND		±50	mA
Package thermal impedance, θ_{JA} ⁽³⁾	DBV package	206	°C/W
	DCK package	252	
	DRL package	142	
Storage temperature range, T_{stg}		–65 to 150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS ⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	V
		$V_{CC} = 3\text{ V}$	2.1	
		$V_{CC} = 5.5\text{ V}$	3.85	
V_{IL}	Low-level Input voltage	$V_{CC} = 2\text{ V}$	5.5	V
		$V_{CC} = 3\text{ V}$	0.9	
		$V_{CC} = 5.5\text{ V}$	1.65	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$	–50	μA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	–4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	–8	
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$	50	μA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	8	
$\Delta t/\Delta v$	Input Transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	20	
T_A	Operating free-air temperature	–40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C		Recommended –40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = –4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.44		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.44		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1		±1	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			1		10		10	µA
C _i	V _I = V _{CC} or GND	5 V		2	10		10		10	pF

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T _A = 25°C		T _A = –40°C to 85°C		Recommended T _A = –40°C to 125°C		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF	5.5	7.9	1	9.5	1	10.5	ns
t _{PHL}				5.5	7.9	1	9.5	1	10.5	
t _{PLH}	A or B	Y	C _L = 50 pF	8	11.4	1	13	1	14	ns
t _{PHL}				8	11.4	1	13	1	14	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 1](#))

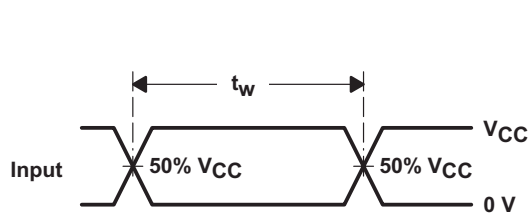
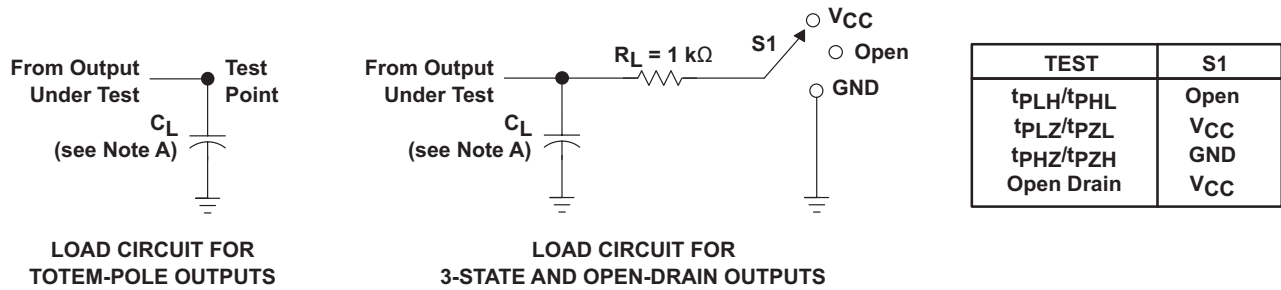
PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T _A = 25°C		T _A = –40°C to 85°C		Recommended T _A = –40°C to 125°C		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A or B	Y	C _L = 15 pF	3.7	5.5	1	6.5	1	7	ns
t _{PHL}				3.7	5.5	1	6.5	1	7	
t _{PLH}	A or B	Y	C _L = 50 pF	5.2	7.5	1	6.5	1	9	ns
t _{PHL}				5.2	7.5	1	6.5	1	9	

OPERATING CHARACTERISTICS

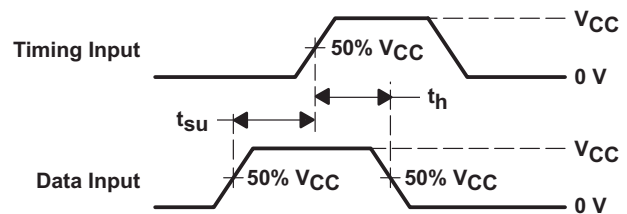
V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance	No load, f = 1 MHz	9.5	pF

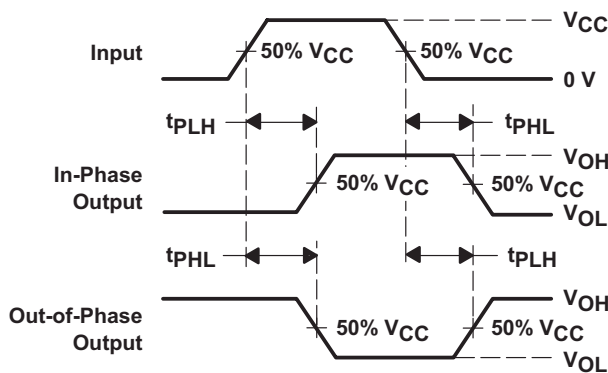
PARAMETER MEASUREMENT INFORMATION



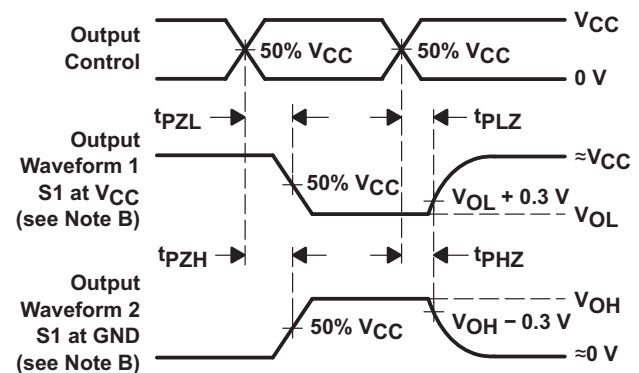
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision M (June 2005) to Revision N	Page
• Changed document format from Quicksilver to DocZone.	1
• Extended operating temperature range to 125°C	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC1G00DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A003 ~ A00G ~ A00L ~ A00S)	Samples
SN74AHC1G00DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A003 ~ A00G ~ A00L ~ A00S)	Samples
SN74AHC1G00DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A003 ~ A00G ~ A00L ~ A00S)	Samples
SN74AHC1G00DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A003 ~ A00G ~ A00L ~ A00S)	Samples
SN74AHC1G00DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A003 ~ A00G ~ A00L ~ A00S)	Samples
SN74AHC1G00DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AA3 ~ AAG ~ AAL ~ AAS)	Samples
SN74AHC1G00DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AA3 ~ AAG ~ AAL ~ AAS)	Samples
SN74AHC1G00DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AA3 ~ AAG ~ AAL ~ AAS)	Samples
SN74AHC1G00DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AA3 ~ AAG ~ AAL ~ AAS)	Samples
SN74AHC1G00DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AA3 ~ AAG ~ AAL ~ AAS)	Samples
SN74AHC1G00DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AAB ~ AAS)	Samples
SN74AHC1G00HDCK3	LIFEBUY	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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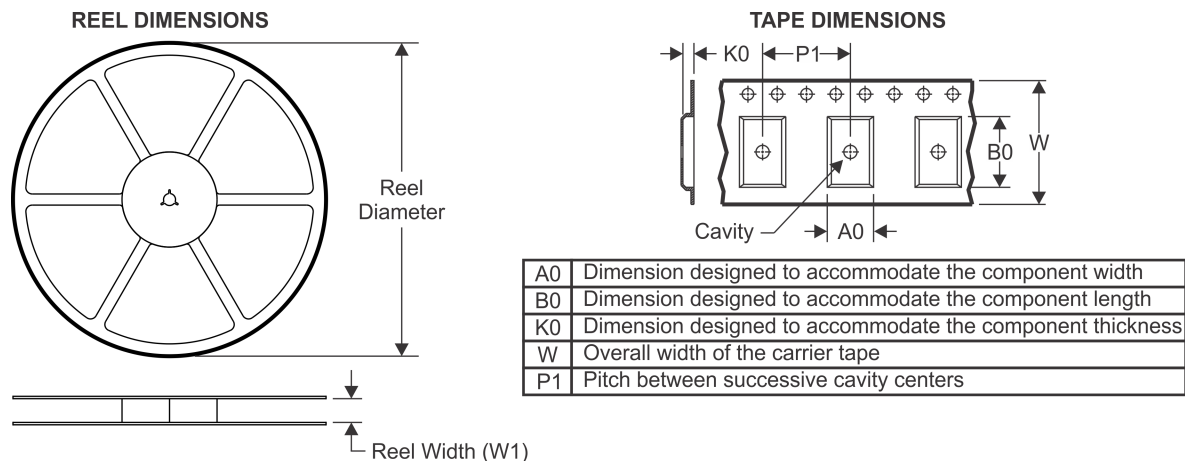
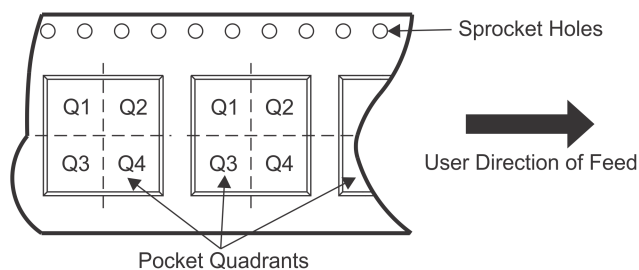
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OTHER QUALIFIED VERSIONS OF SN74AHC1G00 :

- Automotive: [SN74AHC1G00-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74AHC1G00DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G00DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AHC1G00DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G00DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G00DRLR	SOT	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AHC1G00DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

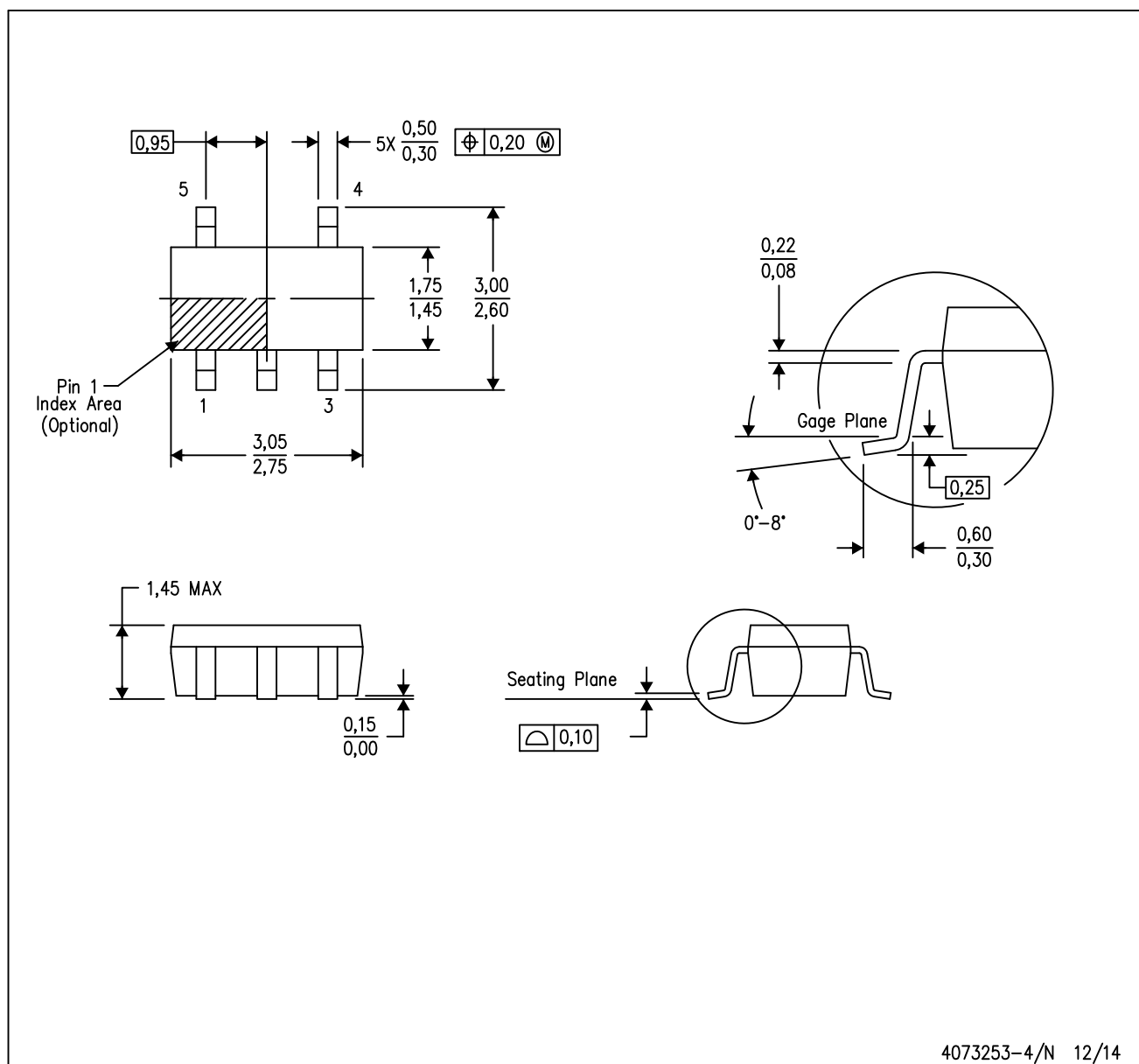


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
SN74AHC1G00DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G00DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74AHC1G00DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G00DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G00DRLR	SOT	DRL	5	4000	184.0	184.0	19.0
SN74AHC1G00DRLR	SOT	DRL	5	4000	202.0	201.0	28.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

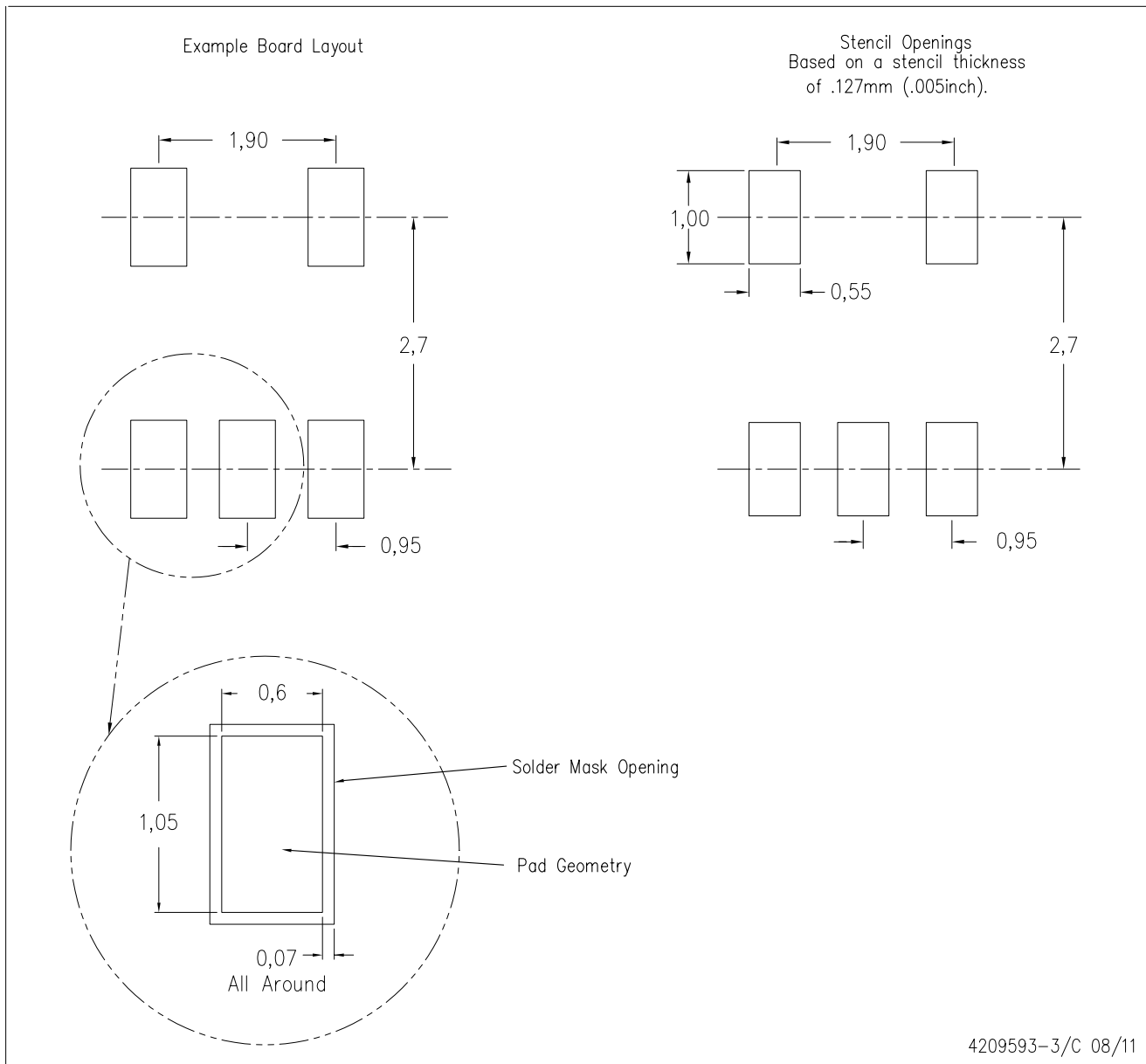


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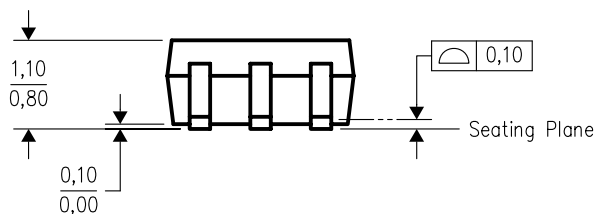
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

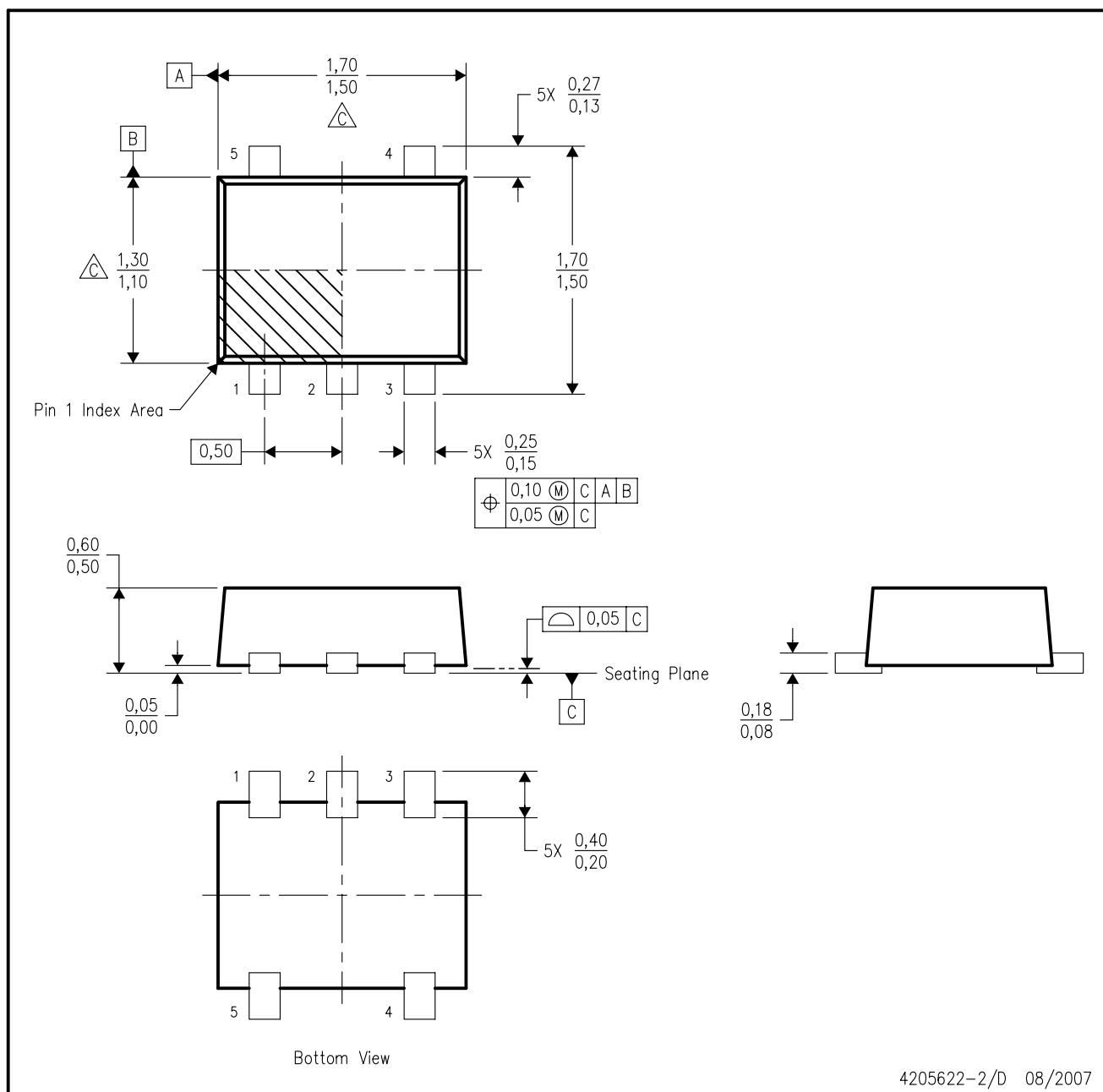
DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.





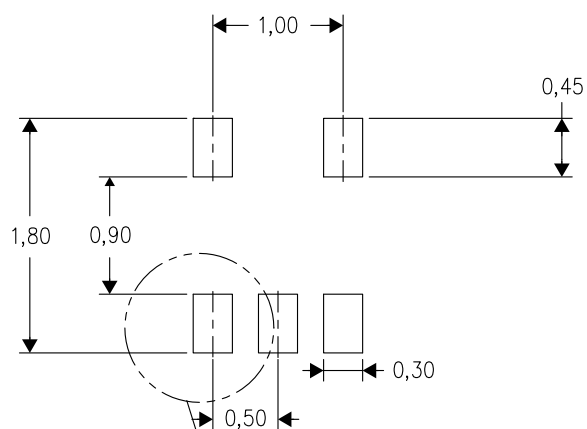
4205622-2/D 08/2007

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.

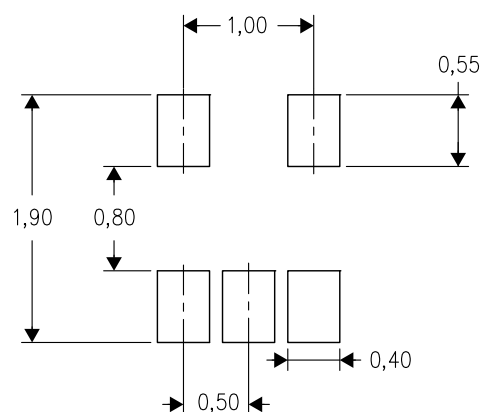
DRL (R-PDSO-N5)

PLASTIC SMALL OUTLINE

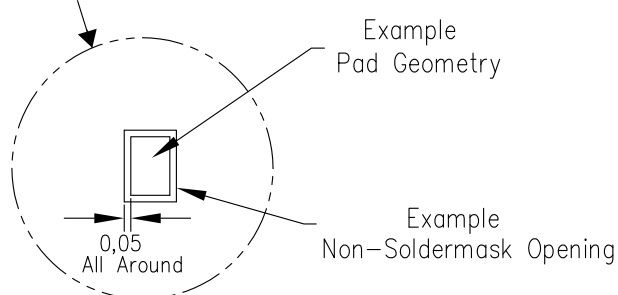
Example Board Layout



Example Stencil Design
(Note E)



Example
Non-Soldermask Defined Pad



4208207-2/E 06/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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