

Renesas Low Power SRAM

Renesas Technology Corp.

SRAM EEPROM Design Dept.

Standard Product Business Group

<http://www.renesas.com/eng/products/memory/index.html>

July, 2009

Low Power SRAM Application

Easy to Use : Work memory

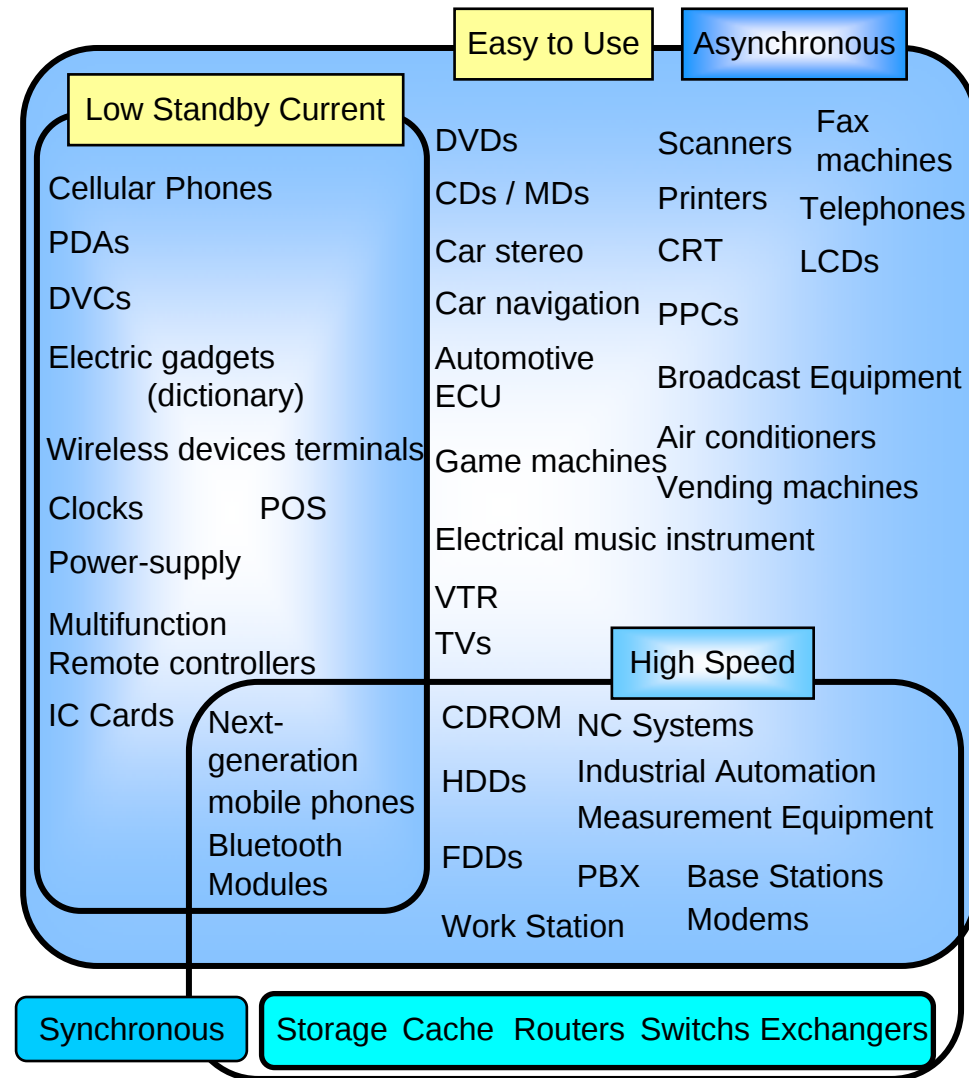
- Work memory for simple timing system
- Main memory for small system or little volume system

Low Standby Current : Battery backup memory

- Backup memory to hold data for a long period of time by sharing battery of mobile phone and device
- Backup Memory driven by battery for sudden system power off

Others

- Memory for 5 V system
- No limitation Memory in write frequency



Advantage of RENESAS Low Power SRAM

<1> Stable supply and long term support

Business strategy	➤	Stable supply and long term support
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<2> Full lineup for many application fields

Supply Voltage	➤	5 V, 3 V
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Density	➤	256 Kbits, 1 Mbit, 2 Mbits, 4 Mbits, 8 Mbits, 16 Mbits, 32 Mbits, 64 Mbits
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Package	➤	SOP, TSOP, sTSOP, μ TSOP, FBGA (CSP)
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<3> Contribution with system performance

Standby current	➤	0.05 μ A (256 Kbits), 0.1 μ A (1 Mbit), 0.5 μ A (4 Mbits), 0.5 μ A (16 Mbits)
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Wide temp.	➤	-40 to +85°C Up to 85°C are individually corresponding
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<4> Next generation technology

High reliability	➤	0.13 μ m 16 Mbits: low soft error by on-chip ECC
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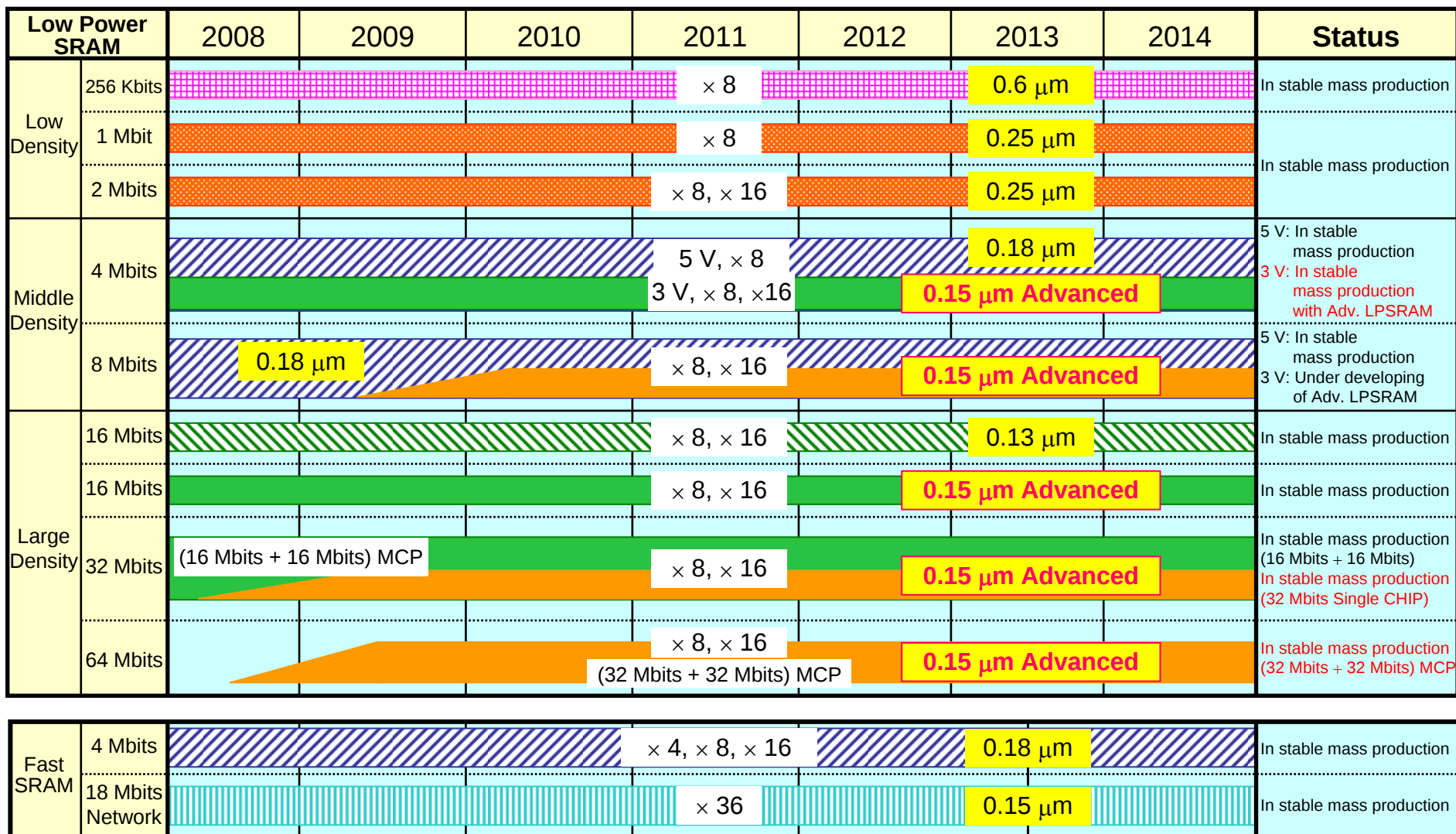
Advanced LPSRAM	➤	New type memory cell which merged SRAM and DRAM capacity
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<5> Environment

Lead free	➤	Switchover for au parts completed in 2005, mass production in preparation
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Standard SRAM Road Map

As of Feb. 2009



Low Density (256 Kbits, 1 Mbit, 2 Mbits) Series

- Low typical standby current under 0.05 μA (256 Kbits)
- Long term production over 22 years (256 Kbits)
- Will continue keeping production stable

Still Stable Support!



Density	Type	Voltage	Package	Access time
256 Kbits	M5M5256D Series	5 V 3.3 V	SOP, TSOP (sTSOP size)	55 ns/70 ns
1 Mbit	M5M51008D, M5M5V108D Series	5 V 3.3 V	SOP, TSOP, sTSOP	55 ns/70 ns
2 Mbits	M5M5V208A, M5M5V216A Series	3.3 V	TSOP, sTSOP	55 ns/70 ns

256-Kbit Low Power SRAM Features and Specification

- M5M5256D Series -

- Fast access time
 - 55 ns max.
- Low current dissipation
 - Active: 30 mA typ./
50 mA max. @55 ns cyc.
 - Standby: 0.05 μ A typ./
5 μ A max. for XL-Version
- Package lineup
 - 28-pin SOP, 1.27-mm pitch
(11.93 $\times$ 17.5 mm)
 - 28-pin TSOP, 0.55-mm pitch
(8.0 $\times$ 13.4 mm)
- New lineup for Wide Voltage version
 - Can be covered for 3.3-V system with wide voltage
(3.0 to 3.6 V and 4.5 to 5.5 V)

Density	256 Kbits (32 Kbits × 8)							
Part No.	M5M5256DFP M5M5256DVP		M5M5256DFP-70LLI M5M5256DVP-70LLI		M5M5256DFP-xG M5M5256DVP-xG		M5M5256DFP-70GI M5M5256VPP-70GI	
Supply voltage	5-V Version: 4.5 to 5.5 V				Wide Version: 3.0 to 3.6 V and 4.5 to 5.5 V			
Access time	55/70 ns		70 ns		70 ns		70 ns	
Active supply current	50 mA max. (Vcc = 5.5 V)				25 mA max. (Vcc = 3.6 V)			
Standby current	LL-Ver.	20 μA max.	40 μA max.		G-Ver.	12 μA max (Vcc = 3.6 V)	24 μA max. (Vcc = 3.6 V)	
	XL-Ver.	5 μA max.	-		XG-Ver.	2.4 μA max (Vcc = 3.6 V)	-	
Power down supply current (Vcc = 3.0 V)	LL-Ver.	10 μA max.	20 μA max.		G-Ver.	10 μA max.	20 μA max.	
	XL-Ver.	2 μA max.	-		XG-Ver.	2 μA max.	-	
Operating temperature	0 to +70°C		-40 to +85°C		0 to +70°C		-40 to +85°C	
Package	SOP-28 pins, TSOP-28 pins (sTSOP size)							

1-Mbit Low Power SRAM Features and Specification

- M5M51008D, M5M5V108D Series -

☐ Wide voltage range operation

- 2.7 to 3.6 V, 4.5 to 5.5 V

☐ Fast access time

- 55 ns max.
@Vcc = 4.5 to 5.5 V
- 70 ns max.
@Vcc = 2.7 to 3.6 V

☐ Rich package lineup

- 32-pin SOP, 1.27-mm pitch (14.1 × 20.75 mm)
- 32-pin TSOP, 0.5-mm pitch (8.0 × 20.0 mm)
- 32-pin sTSOP, 0.5-mm pitch (8.0 × 13.4 mm)

Density	1 Mbit (128 Kbits × 8)			
Part No.	M5M51008DFP M5M51008DVP M5M51008DRV M5M51008DKV	M5M51008DFP-xxHI M5M51008DVP-xxHI M5M51008DRV-xxHI M5M51008DKV-xxHI	M5M5V108DFP M5M5V108DVP M5M5V108DKV	M5M5V108DFP-70HI M5M5V108DVP-70HI M5M5V108DKV-70HI
Supply voltage	4.5 to 5.5 V		2.7 to 3.6 V	
Access time	55/70 ns		70 ns	
Active supply current	85 mA max.		35 mA max.	
Standby current	20 µA max.	40 µA max.	12 µA max.	24 µA max.
Power down supply current (Vcc = 3.0 V)	10 µA max.	20 µA max.	10 µA max.	20 µA max.
Operating temperature	0 to +70°C	-40 to +85°C	0 to +70°C	-40 to +85°C
Package	SOP-32 pins/TSOP-32 pins/sTSOP-32 pins			

2-Mbit Low Power SRAM Features and Specification

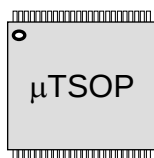
- M5M5V208A, M5M5V216A Series -

- Fast access time
 - 55 ns max.
- Low current dissipation
 - Active: 20 mA typ./25 mA max.
@f = 10 MHz
 - Standby: 0.3 μ A typ./30 μ A max.
- Small Package lineup
 - 32-pin sTSOP, 0.5-mm pitch
(8.0 $\times$ 13.4 mm) for $\times$ 8 devices

Density	2 Mbits (256 Kbits $\times$ 8)	2 Mbits (128 Kbits $\times$ 16)
Part No.	M5M5V208AKV-55HI M5M5V208AKV-70HI	M5M5V216ATP-55HI M5M5V216ATP-70HI
Supply voltage	2.7 to 3.6 V	
Access time	55/70 ns	
Active supply current	25 mA max. (f = 10 MHz)	60 mA max. (f = 10 MHz)
Standby current	30 μ A max.	30 μ A max.
Power down supply current (Vcc = 2.0 V)	24 μ A max.	24 μ A max.
Operating temperature	-40 to +85°C	
Package	sTSOP-32 pins	TSOP-44 pins

Middle Density (4 Mbits, 8 Mbits) Series

More Market Movement!



- 5 V Support
- Rich Package Lineup
- Will continue keeping production stable

Density	Type	Voltage	Package	Access time
4 Mbits	• R1LP0408C, R1LV0408D, R1LV0416D, R1LV0414D Series	5 V, 3.3 V	SOP, TSOP, sTSOP, FBGA	55/70 ns
8 Mbits	• M5M5W816, M5M5W817	3.3 V	μTSOP, TSOP, FBGA	55/70 ns
	• HM628100, HM6216514, HM62V8100 Series	5.5 V, 3.3 V	TSOP	55 ns

4-Mbit Low Power SRAM Specification

- C and D-Mask

R1LP0408C, R1LV0408D, R1LV0416D, R1LV0414D Series

High productivity products

❑ Adoption of the 0.15-μm 6 Tr Memory Cells

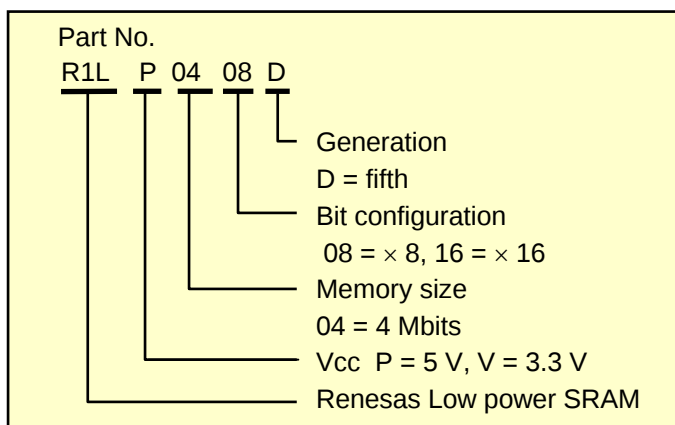
❑ Wide voltage range operation
2.7 to 3.6 V, 4.5 to 5.5 V × 8 devices
2.7 to 3.6 V × 16 devices

❑ Fast access time
55 ns max.

❑ Low current dissipation
Operation: 18 mA typ./25 mA max. @55 ns cyc.
Standby: 10 μA max. for SL-Version

Density		4 Mbits (512 Kbits × 8)				4 Mbits (256 Kbits × 16)
Part No.		R1LP0408C	R1LP0408C -xxl	R1LV0408D	R1LV0408D -xxl	R1LV0416D-xxl R1LV0414D-xxl ¹
Supply voltage		4.5 to 5.5 V		2.7 to 3.6 V		2.7 to 3.6 V
Access time		55/70 ns				55/70 ns
Operating current		25 mA max.				25 mA max.
Standby current	L-Ver.	20 μA max.				20 μA max.
	S-Ver.	10 μA max.				10 μA max.
Data retention current	L-Ver.	20 μA max. (3 V)				20 μA max. (3 V)
	S-Ver.	10 μA max. (3 V)				10 μA max. (3 V)
Operating temperature		-20 to +70°C	-40 to +85°C	0 to +70°C	-40 to +85°C	-40 to +85°C
Package		SOP-32 pins TSOP(II)-32 pins		SOP-32 pins TSOP(II)-32 pins sTSOP-32 pins		FBGA(CSP)-48 balls TSOP(II)-44 pins

*1: One chip-select pin.



8-Mbit Low Power SRAM Specification

- HM628100, HM6216514, HM62V8100,
M5M5W816 and M5M5W817 Series -

- ☐ Adoption of the 0.18-μm CMOS process and 6 MOS Memory Cells
- ☐ Low current dissipation: Standby 0.5 μA typ./10 μA max. for SL-Ver. (Ta = 25°C)
- ☐ Small Package lineup: 52-pin μTSOP, 0.4-mm pitch (10.49 × 10.79 mm)

Density	8 Mbits					
	1 Mbit × 8	512 Kbits × 16	1 Mbit × 8	512 Kbits ×16		1 Mbit × 8/ 512 Kbits × 16
Part No.	HM628100I*1	HM6216514I	HM62V8100I*1	M5M5W816TP	M5M5W816WG	M5M5W817KT*2
Supply voltage	4.5 to 5.5 V		2.7 to 3.6 V			
Access time	55 ns		55 ns	55/70 ns		70 ns
Operating current	30 mA max.	35 mA max.	25 mA max.	50 mA max. (f = 10 MHz)		
Standby current	10 μA max. (SL Ver.)		10 μA max. (SL Ver.)	40 μA max.		
Data retention current	10 μA max. (3 V) (SL Ver.)		10 μA max. (3 V) (SL Ver.)	30 μA max. (2.0 V)		
Operating temperature	-40 to +85°C					
Package	TSOP(II) -44 pins				FBGA (CSP) - 48 balls	μTSOP-52 pins

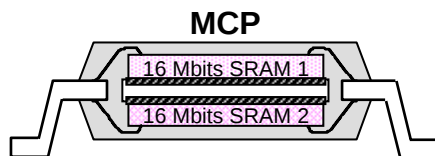
*1: Two chip-select pins.

*2: BYTE# pin controls × 8 mode or × 16 mode.

In case of × 8 mode (BYTE = 'L'), pin 47 is an address pin (A-1).

Large Density (16 Mbits, 32 Mbits, 64 Mbits) Series

The aim is to further expand our SRAM business!



- High performance: 45 ns, on-chip ECC
- Advanced LPSRAM: 16-Mbits and 3.3-V products are in stable mass production
- MCP (Multi Chip Package)

Density	Type	Power Supply Voltage	Package	Access time/Feature
Full CMOS LPSRAM				
16 Mbits	• R1LV1616H Series	3.3 V	TSOP, FBGA	45 ns/55 ns/On-chip ECC
Advanced LPSRAM				
16 Mbits	• R1LV1616R Series	3.3 V	TSOP, μ TSOP, FBGA	(55 ns)*/ 70 ns New type Memory Cell
32 Mbits	• R1WV3216R Series (MCP)	3.3 V	μ TSOP, FBGA	70 ns New type Memory Cell
	• R1LV3216R Series (Single-chip)	3.3 V	TSOP, μ TSOP	55 ns/ 70 ns New type Memory Cell
64 Mbits	• R1WV6416R Series (MCP)	3.3 V	TSOP, μ TSOP, FBGA	55 ns / 70 ns New type Memory Cell

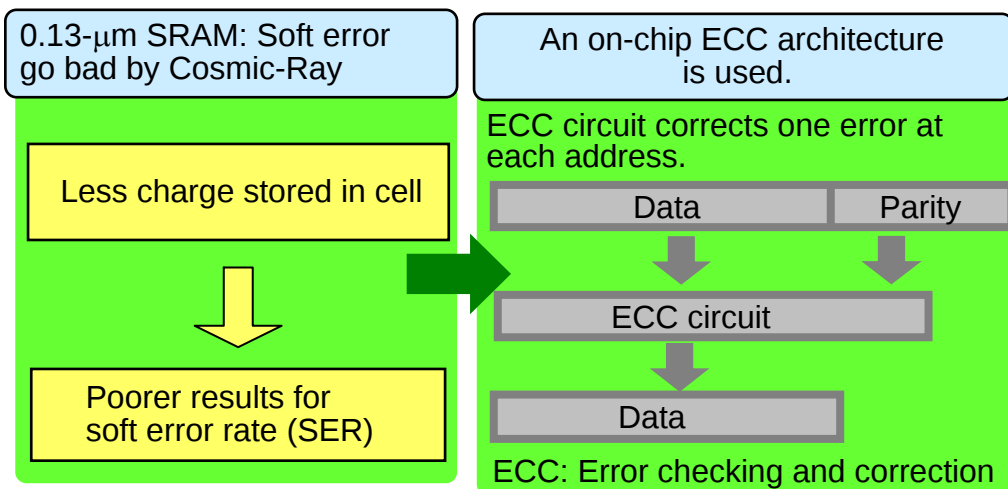
Advanced LPSRAM

*: Please contact each sales office in your region, for inquiries regarding advanced LPSRAM with access time of 55 ns.

16-Mbit Low Power SRAM Specification

- R1LV1616HSA, R1LV1616HBG Series -

- ☐ Adoption of the 0.13-μm CMOS process and 6 Tr Memory Cells
- ☐ Operating voltage
 - 2.7 to 3.6 V
- ☐ Fast access time
 - 45 ns max.
- ☐ Low current dissipation
 - Standby: 0.5 μA typ./8 μA max. for S-Version
- ☐ High reliability
 - Low soft error by on-chip ECC



Density		16 Mbits
		1 Mbit × 16/2 Mbits × 8* ¹
Part No.		R1LV1616HSA R1LV1616HBG
Supply voltage [Vcc]		2.7 to 3.6 V
Operation current		20 mA max.
Access time		45/55 ns
Standby Current [ISB1]	L-Ver.	25 μA max.
	S-Ver.	8 μA max.
Data retention Current [ICCDR]	L-Ver.	25 μA max.
	S-Ver.	8 μA max.
Operating temperature		-40 to +85°C
Package		TSOP(I) -48 pins* ¹ FBGA(CSP) - 48 balls

*1: BYTE# pin controls × 8 mode or × 16 mode.
TSOP products only.

Advanced Technology: What's Advanced LPSRAM?

Advanced low-power SRAM (LPSRAM) is fully compatible with conventional SRAM and has been developed as Renesas' proprietary technology, achieving both even greater reliability and reduced cell areas.

Reduce Cell size :

(1) Stack Load Tr

(2) Scaling down of Drive Tr.

Technology :

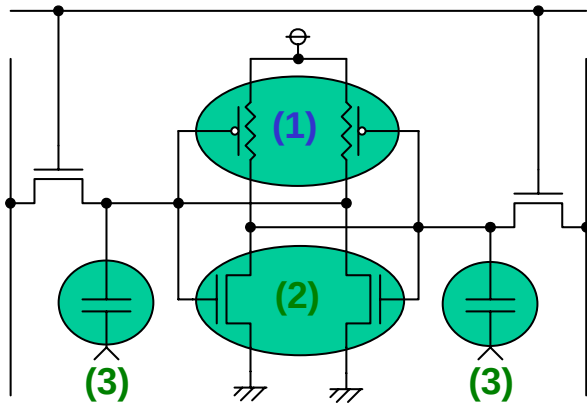
(1) TFT Technology

(3) DRAM Capacitor

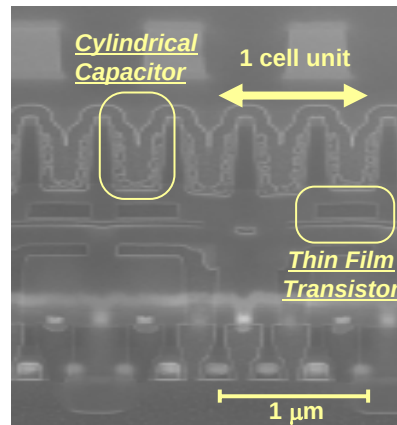
High Reliability :

Latch Up Free

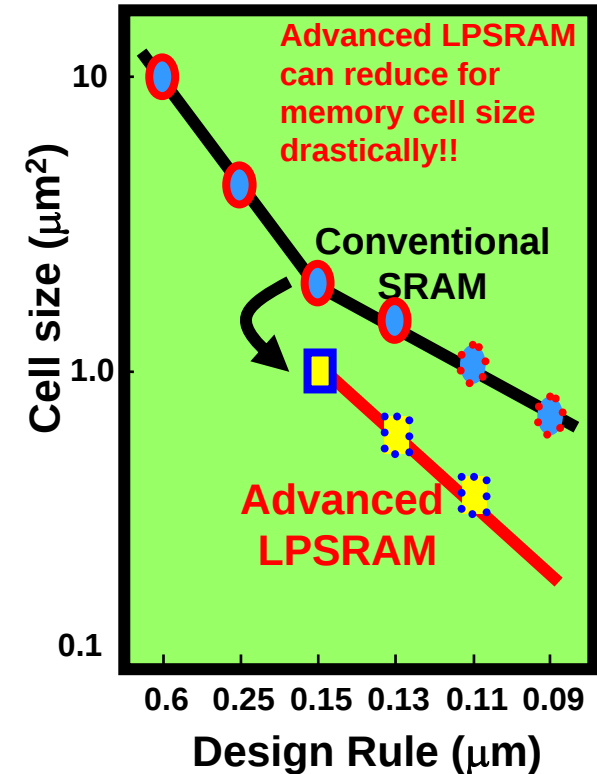
Soft Error Free



< Memory Cell Circuit >



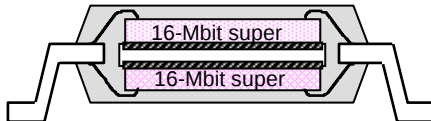
< Cross Section of Memory Cell >



0.15-μm advanced LPSRAM matches the strengths of the conventional 0.11 – to 0.10-μm SRAM cell (full CMOS)!

Features and Specifications: 16-Mbit and 32-Mbit Advanced LPSRAM Product Families

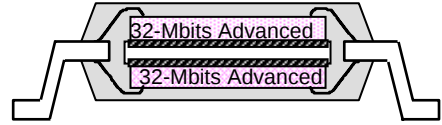
- 0.15- μm CMOS process
Smaller chips (equivalent to half the size of a full CMOS SRAM cell) for more compact packages
- High reliability
Low soft error by capacitor cell

Density	16 Mbit (2 Mbits $\times$ 8/1 Mbit $\times$ 16) ^{*1}	32 Mbit (4 Mbits $\times$ 8/2 Mbits $\times$ 16) ^{*1} 16 Mbits + 16 Mbits Stacked MCP
Part No.	R1LV1616RSA/RSD/RBG	R1WV3216RSD/RBG
Supply voltage (Vcc)	2.7 V to 3.6 V	←
Access time	(55) /70 ns	70 ns
Active current	25 mA typ. @3.0 V, 25°C	30 mA typ. @3.0 V, 25°C
Data retention current	2 μA typ. @3.0 V, 25°C	4 μA typ. @3.0 V, 25°C
Operating temperature	R: 0 to 70°C, I: -40 to 85°C	
Shipping type (chip/wafer, package)	1. Shipment as chips or wafers 2. Compact packages: 52- μTSOP , 48-FBGA 3. Packaging facility: 48-TSOP (I)	MCP (μTSOP and FBGA) The same package as the 16-Mbit product 

*1: TSOP and μTSOP can be possible to switch over $\times 8/\times 16$. for $\times 8$, the BYTE# signal is fixed low and the A-1 address bit is assigned to pin 47.

Features and Specifications: 32-Mbit and 64-Mbit Advanced LPSRAM Product Families

Under
Development

Density	32 Mbits (4 Mbits × 8/2 Mbits × 16)* ¹ 32 Mbits single-chip type	64 Mbits (8 Mbits × 8/4 Mbits × 16)* ¹ 32 Mbits + 32 Mbits stacked MCP type
Part No.	R1LV3216RSA/RSD	R1WV6416RSA/RSD/RBG
Supply voltage [VCC]	2.7 V to 3.6 V	←
Access time	55/70 ns	55/70 ns
Operating current	40 mA typ. @ 3.0 V, 25°C	45 mA typ. @ 3.0 V, 25°C
Data retention current	4 μA typ. @ 3.0 V, 25°C	8 μA typ. @ 3.0 V, 25°C
Operating temperature	“R”: 0 to 70°C, “I”: -40 to 85°C	
Package	1. Shipment as chips or wafers 2. Compact packages: 52-μTSOP 3. Packaging facility: 48-TSOP (I)	MCP (52-μTUOP, 48-TSOP (I), 48-FBGA) 

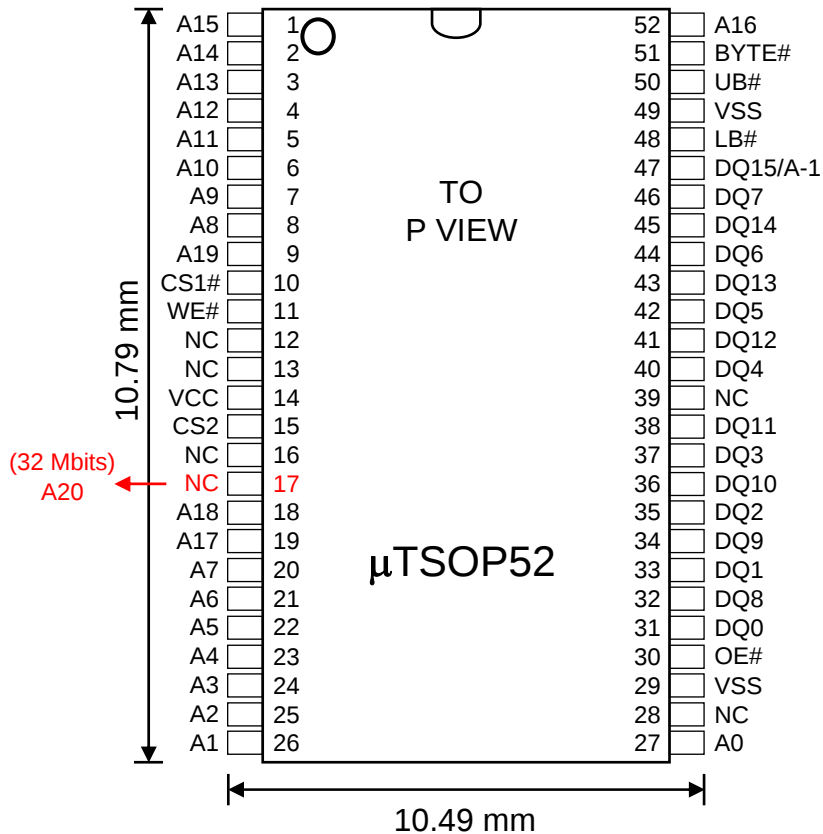
*1: TSOP and μTSOP can be possible to switch over ×8/×16. For × 8, the BYTE# signal is fixed low and the A-1 address bit is assigned to pin 47.

16-Mbit/32-Mbit (16 Mbits + 16 Mbits MCP) Advanced LPSRAM Package Lineup

- R1LV1616R, R1LA1616R, R1WV3216R Series -

µTSOP

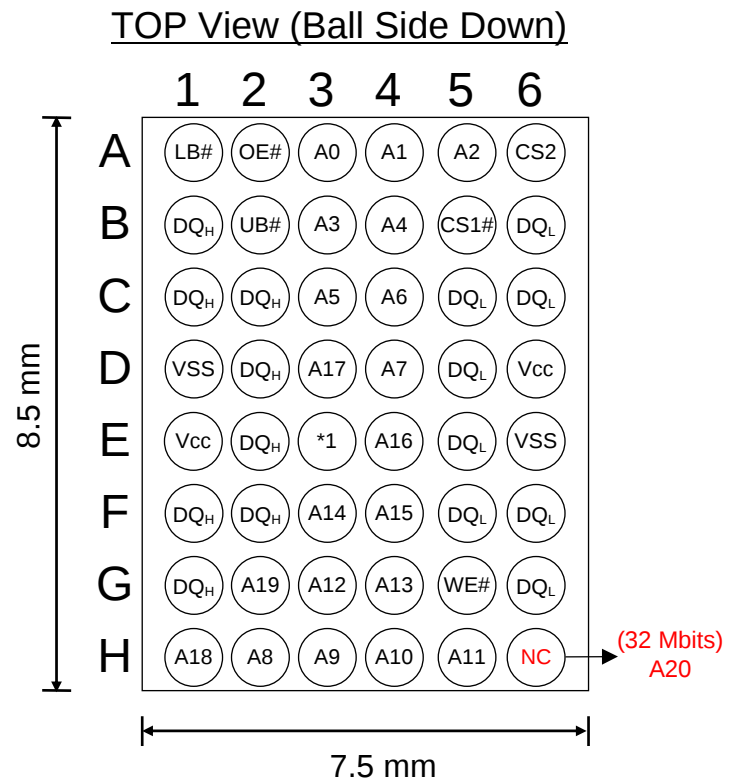
Pin pitch: 0.4 mm



Remark: BYTE# pin controls × 8 mode or × 16 mode.
In case of × 8 mode (BYTE = 'L'), pin 47 is an address pin (A-1).

FBGA

Ball pitch: 0.75 mm



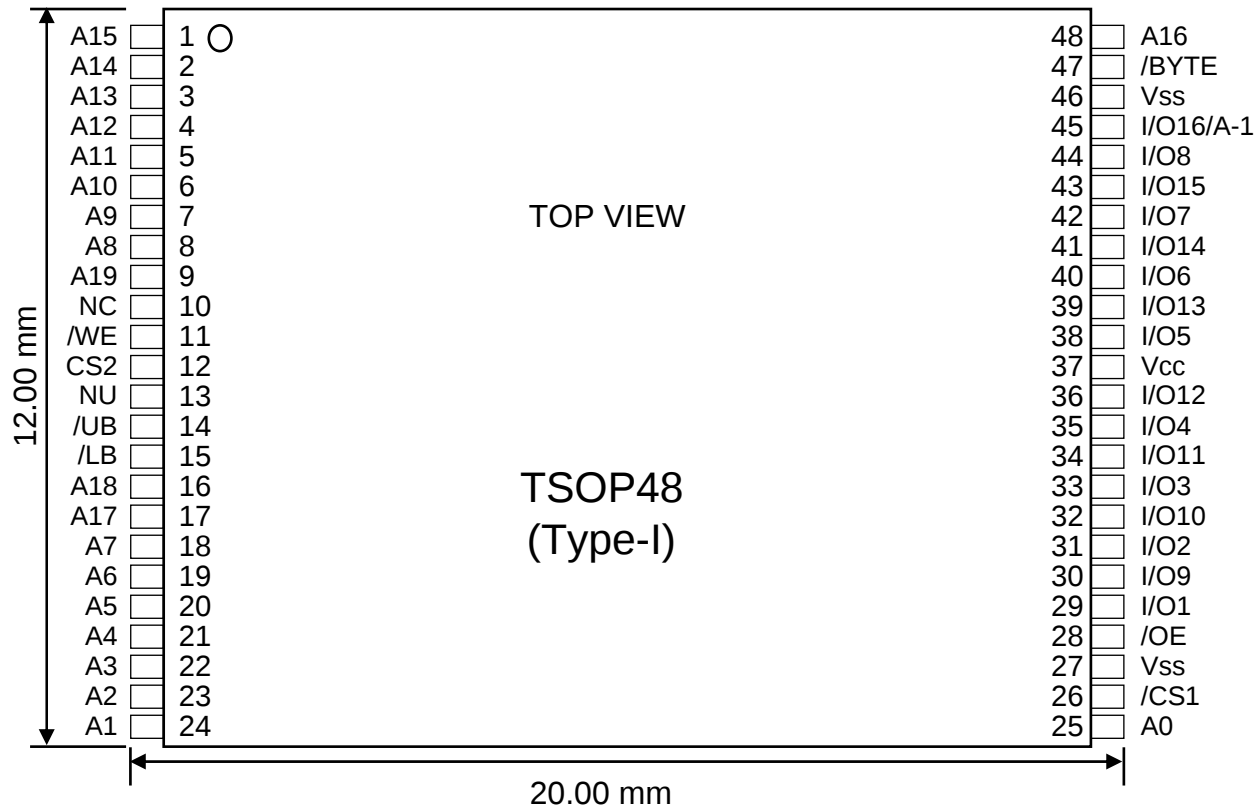
*1 : VSS or NC

16-Mbit Advanced LPSRAM: 48-pin TSOP Package Lineup

- R1LV1616RSA Series -

TSOP

Pin pitch: 0.5 mm



Remark: BYTE# pin controls × 8 mode or × 16 mode.

In case of × 8 mode (BYTE = 'L'), pin 45 is an address pin (A-1).

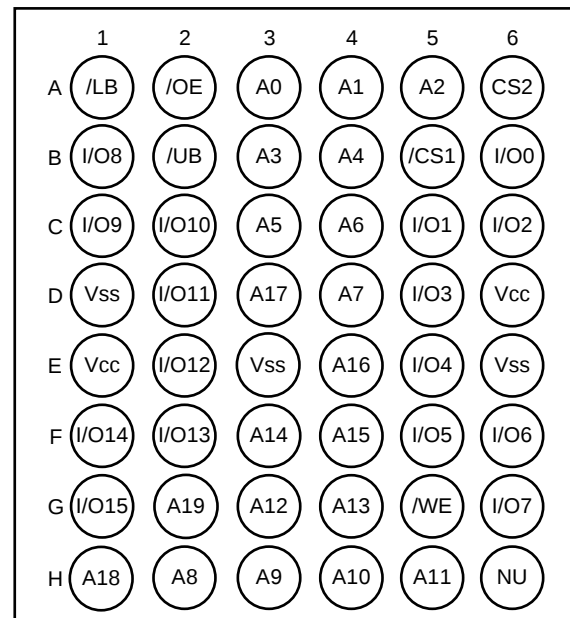
16-Mbit Low Power SRAM FBGA (CSP) Package

- R1LV1616HBG Series -

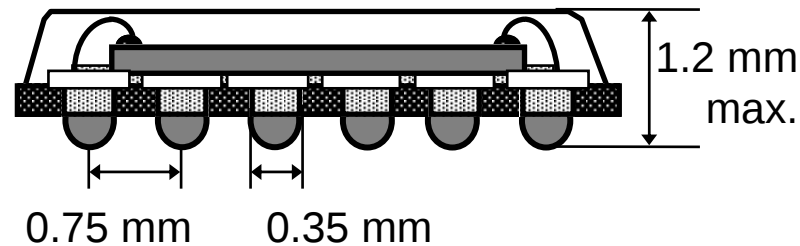
Features

- Package size :
8.0 × 9.5 mm
- Package height: 1.2 mm max.
- Ball counts: 48 balls
- Ball pitch: 0.75 mm
- Ball diameter: $\phi 0.35$ mm

TOP View (Ball Side Down)



NU: Not used (Test mode pin)
Must be connected to ground (Vss)
or not be connected (Open).

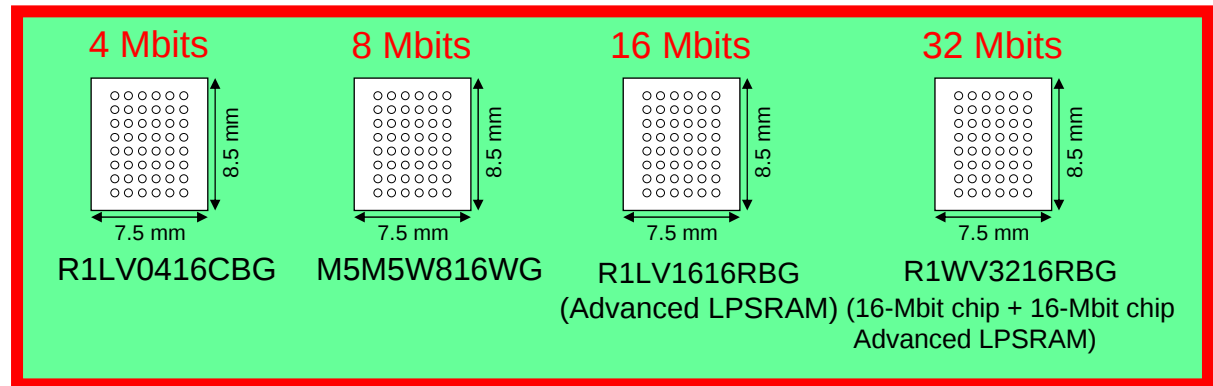


Upward compatibility with 4-Mbit/8-Mbit/16-Mbit/32-Mbit FBGA (CSP)

Realized upper compatibility with 4-Mbit, 8-Mbit, 16-Mbit, 32-Mbit

TOP View (Ball Side Down)

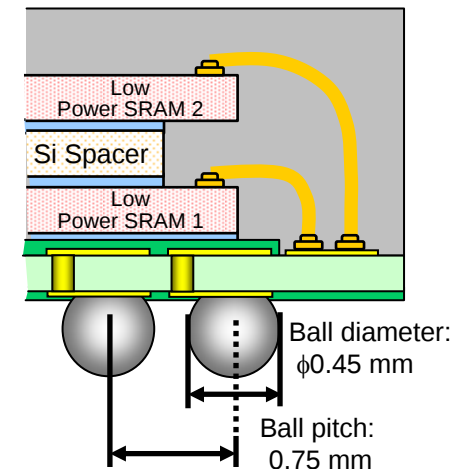
	1	2	3	4	5	6
A	$\overline{\text{BC}}1$	$\overline{\text{OE}}$	A0	A1	A2	S2
B	DQ _H	$\overline{\text{BC}}2$	A3	A4	$\overline{\text{SI}}$	DQ _L
C	DQ _H	DQ _H	A5	A6	DQ _L	DQ _L
D	GND	DQ _H	A17	A7	DQ _L	V _{CC}
E	V _{CC}	DQ _H	GND	A16	DQ _L	GND
F	DQ _H	DQ _H	A14	A15	DQ _L	DQ _L
G	DQ _H	**	A12	A13	$\overline{\text{W}}$	DQ _L
H	*	A8	A9	A10	A11	***



Ball Assignments of upper address

	H1 (*)	G2 (**)	H6 (***)
4 Mbits	NC	NC	NC
8 Mbits	A18	NC	NC
16 Mbits	A18	A19	NC
32 Mbits	A18	A19	A20

→ Compatible with other vendors

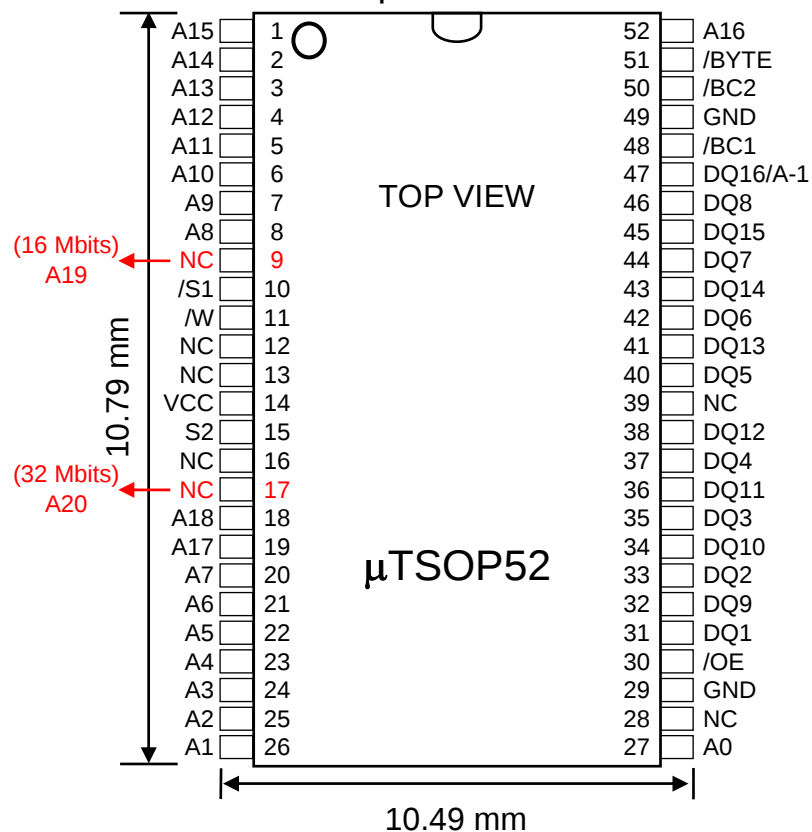


TSOP Package Pin Arrangement

× 8 or × 16 configuration is controlled by /Byte pin set

8-/16-/32-Mbit Low power SRAM
(M5M5W817/R1LV1616R/R1WV3216R)

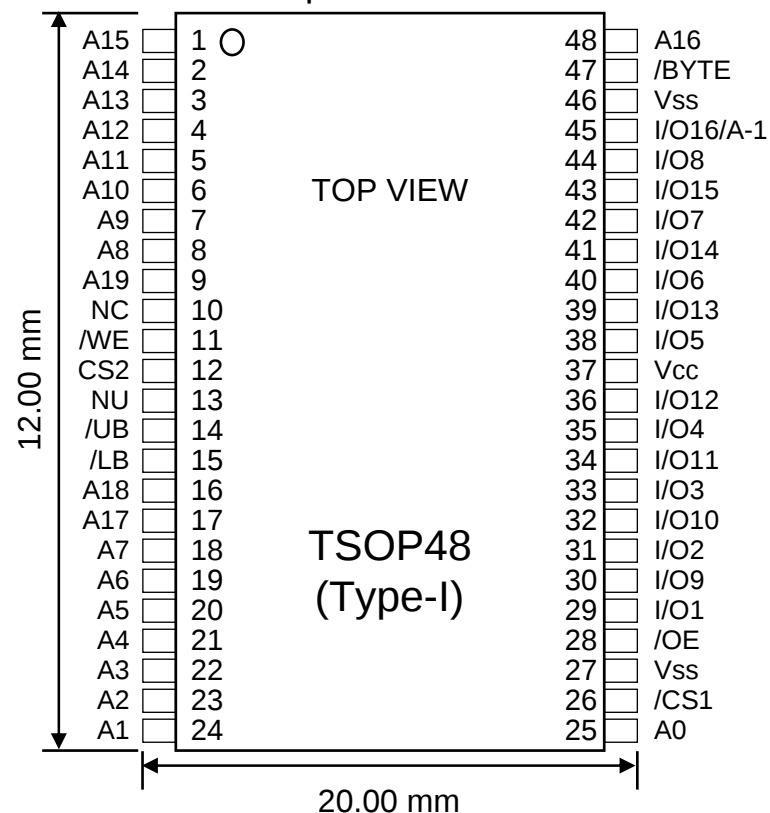
Pin pitch: 0.4 mm



Remark: BYTE# pin controls × 8 mode or × 16 mode.
In case of × 8 mode (BYTE = 'L'), pin 47 is an address pin (A-1).

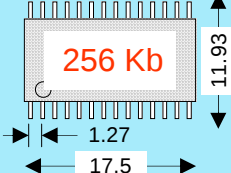
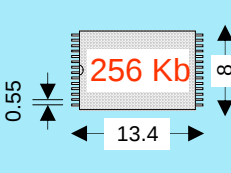
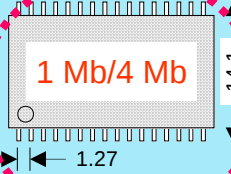
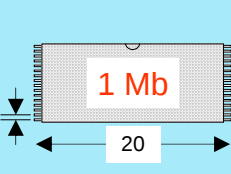
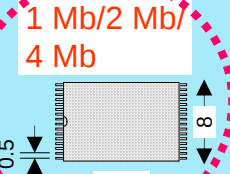
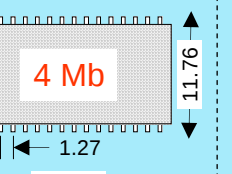
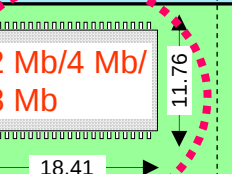
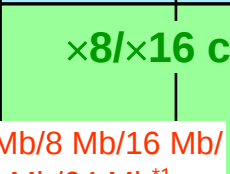
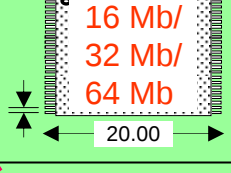
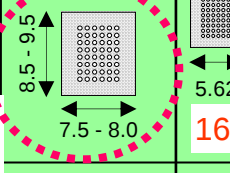
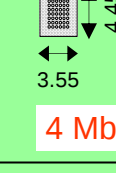
16-Mbit Low power SRAM
(R1LV1616RSA/R1LV1616HSA)

Pin pitch: 0.5 mm



Remark: BYTE# pin controls × 8 mode or × 16 mode.
In case of × 8 mode (BYTE = 'L'), pin 45 is an address pin (A-1).

Low Power SRAM Package Lineup

	SOP	TSOP(I)	sTSOP(I)	TSOP(II)	μTSOP(II)	FBGA	Wafer Level-CSP
28 pins							
32 pins							
44 pins							
48 pins (48 ball)							
52 pins							

×8 config. ↑

×8/×16 config. ↓

Renesas provides 6 kinds of packages which have upper-compatibility on pin configuration.
So it's easy to expand density without changing PCB.

*1: Package size for 64 Mb FBGA is 8.5 mm × 11 mm

Low Power SRAM Lineup (1)

256 Kbits

Supply voltage	Part number	Bit config.	Package				Status
			DIP	SOP	TSOP	sTSOP	
4.5 V - 5.5 V	M5M5256D	32 Kbits × 8	-	√	√	-	M.P
3.0 V - 3.6 V 4.5 V - 5.5 V	M5M5256D - xG	32 Kbits × 8	-	√	√	-	M.P

1 Mbit

Supply voltage	Part number	Bit config.	Package				Status
			DIP	SOP	TSOP	sTSOP	
4.5 V - 5.5 V	M5M51008D	128 Kbits × 8	-	√	√	√	M.P
2.7 V - 3.6 V	M5M5V108D	128 Kbits × 8	-	√	√	√	M.P

2 Mbits

Supply voltage	Part number	Bit config.	Package				Status
			SOP	TSOP	sTSOP	TSOP-II	
2.7 V - 3.6 V	M5M5V208A	256 Kbits × 8	-	-	√	-	M.P
2.7 V - 3.6 V	M5M5V216A	128 Kbits × 16	-	-	-	√	M.P

4 Mbits

Supply voltage	Part number	Bit config.	Package				Remark	Status
			DIP	SOP	TSOP-II	sTSOP		
4.5 V - 5.5 V	R1LP0408C	512 Kbits × 8	-	√	√	-		M.P
2.7 V - 3.6 V	R1LV0408D	512 Kbits × 8	-	√	√	√		M.P

Supply voltage	Part number	Bit config.	Package		Remark	Status
			TSOP-II	FBGA (CSP)		
2.7 V - 3.6 V	R1LV0416D	256 Kbits × 16	√	√	With two CS input pins	M.P
2.7 V - 3.6 V	R1LV0414D	256 Kbits × 16	√	-	With one CS pin	M.P

Low Power SRAM Lineup (2)

8 Mbits

Supply voltage	Part number	Bit config.	Package			Remark	Status
			TSOP- II	FBGA (CSP)	μTSOP		
2.7 V - 3.6 V	HM62V8100I	1 Mbit × 8	√	-	-	Supporting "SL" version	M.P
4.5 V - 5.5 V	HM628100I	1 Mbit × 8	√	-	-	Supporting "SL" version	M.P
	HM6216514I	512 Kbits × 16	√	-	-	Supporting "SL" version	M.P
2.7 V - 3.6 V	M5M5W816	512 Kbits × 16	√	√	-		M.P
	M5M5W817	512 Kbits × 16 1 Mbit × 8	-	-	√	Byte control for ×8/×16 switch	M.P

16 Mbits

Supply voltage	Part number	Bit config.	Package			Remark	Status
			TSOP- II	FBGA (CSP)	μTSOP		
2.7 V - 3.6 V	R1LV1616H	2 Mbits × 8 1 Mbits × 16	√	√	-	Byte control for ×8/×16 switch	M.P

16 Mbits Advanced

Supply voltage	Part number	Bit config.	Package			Remark	Status
			TSOP- I	μTSOP	FBGA (CSP)		
2.7 V - 3.6 V	R1LV1616R	2 Mbits × 8 1 Mbit × 16	√	√	√	TSOP and μTSOP: Byte control for ×8/×16 switch FBGA: ×16	M.P

32 Mbits Advanced

Supply voltage	Part number	Bit config.	Package			Remark	Status
			TSOP- I	μTSOP	FBGA (CSP)		
2.7 V - 3.6 V	R1WV3216R (MCP type)	4 Mbits × 8 2 Mbits × 16	-	√	√	μ SOP: Byte control for ×8/×16 switch FBGA: ×16	M.P
	R1LV3216R (Single-chip type)	4 Mbits × 8 2 Mbits × 16	√	√	-	TSOP and μTSOP: Byte control for ×8/×16 switch	Under development

64 Mbits Advanced: (32 Mbits chip + 32 Mbits chip)

Supply voltage	Part number	Bit config.	Package			Remark	Status
			TSOP- I	μTSOP	FBGA (CSP)		
2.7 V - 3.6 V	R1WV6416R (MCP type)	8 Mbits × 8 4 Mbits × 16	√	√	√	TSOP and μTSOP: Byte control for ×8/×16 switch FBGA: ×16	Under development



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