LMC6482 CMOS Dual Rail-to-Rail Input and Output Operational Amplifier

1 Features

- Specifications are typical unless otherwise noted
- Rail-to-rail input common-mode voltage range (specified over temperature)
- Rail-to-rail output swing (within 20-mV of supply rail, 100-kΩ load)
- Specified 3-V, 5-V, and 15-V performance
- Excellent CMRR and PSRR: 82 dB
- Ultra-low input current: 20 fA
- High voltage gain (RL = 500 kΩ): 130 dB
- Specified for 2-kΩ and 600-Ω loads
- Power-good output
- Packages: PDIP, SOIC, and VSSOP

2 Applications

- Data acquisition (DAQ)
- Currency counter
- Oscilloscope (DSO)
- Intra-DC interconnect (METRO)
- Macro remote radio unit (RRU)
- Multiparameter patient monitor
- Merchant telecom rectifiers
- Train control and management
- Process analytics (pH, gas, concentration, force, and humidity)
- Three phase UPS
- Improved replacement for TLC272, TLC277

3 Description

The LMC6482 device provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes this device unique among rail-to-rail input amplifiers. The device is an excellent choice for systems, such as data acquisition, that require a large input signal range. The LMC6482 is also an excellent upgrade for circuits using limited common-mode range amplifiers, such as the TLC272 and TLC277.

Maximum dynamic signal range is provided in low voltage and single supply systems by the rail-to-rail output swing of the LMC6482. The rail-to-rail output swing is maintained for loads down to 600 Ω of the device. Specified low-voltage characteristics and low-power dissipation make the LMC6482 a great choice for battery-operated systems.

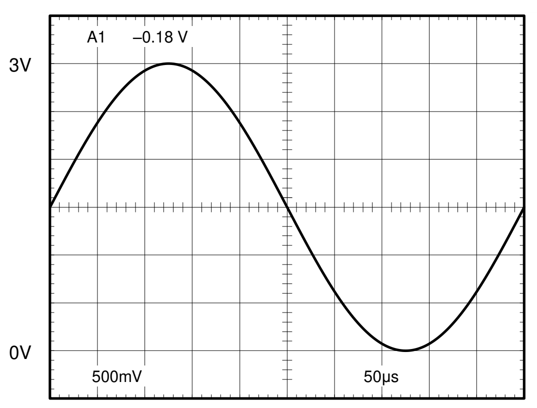
The LMC6482 is available in 8-pin PDIP and SOIC packages. The device is also available in a VSSOP package, almost half the size of a SOIC-8 device. See the LMC6484 for a quad CMOS operational amplifier with these same features.

Device Information(1)

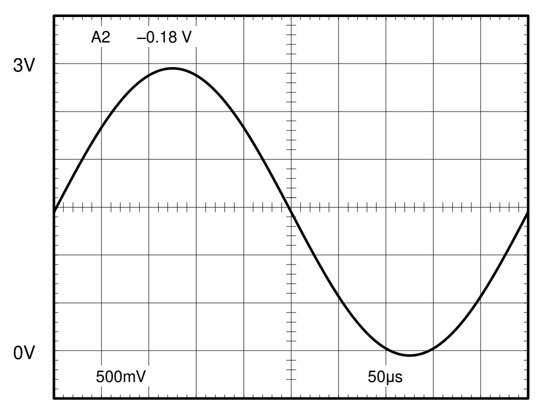
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMC6482	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Rail-to-Rail Input



Rail-to-Rail Output



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (April 2020) to Revision G **Page**

- Deleted old note 4 from *Electrical Characteristics for $V^+ = 5$ V* table. 4

Changes from Revision E (April 2015) to Revision F **Page**

- Changed junction temperature max value from –85°C to 85°C (typo) in *Recommended Operating Conditions* table.......... 4

Changes from Revision D (March 2013) to Revision E **Page**

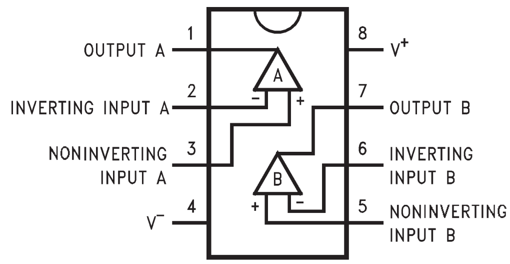
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision C (March 2013) to Revision D **Page**

- Changed layout of National Semiconductor Data Sheet to TI format 27

5 Pin Configuration and Functions

D, DGK, and P Packages
8-Pin SOIC, VSSOP, and PDIP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	OUTPUT A	O	Output for Amplifier A
2	INVERTING INPUT A	I	Inverting input for Amplifier A
3	NONINVERTING INPUT A	I	Noninverting input for Amplifier A
4	V^-	P	Negative supply voltage input
5	NONINVERTING INPUT B	I	Noninverting input for Amplifier B
6	INVERTING INPUT B	I	Inverting input for Amplifier B
7	OUTPUT B	O	Output for Amplifier B
8	V^+	P	Positive supply voltage input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
	Differential input voltage		±Supply Voltage	
	Voltage at input/output pin	$(V^-) - 0.3$	$(V^+) + 0.3$	V
	Supply voltage $(V^+ - V^-)$		16	V
	Current at input pin (3)	−5	5	mA
	Current at output pin(4)(5)	–30	30	mA
	Current at power supply pin		40	mA
	Lead temperature (soldering, 10 sec.)		260	°C
	Junction temperature (6)		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
(4) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.
(5) Do not short circuit output to V^+, when V^+ is greater than 13 V or reliability will be adversely affected.
(6) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Supply voltage		3	15.5	V
	Junction temperature	LMC6482AM	–55	125	°C
		LMC6482AI, LMC6482I	–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.4 Thermal Information

THERMAL METRIC (1)		LMC6482 D (SOIC) 8 PINS	LMC6482 DGK (VSSOP) 8 PINS	LMC6482 P (PDIP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	155	194	90	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for V^+ = 5 V

unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	T_J = 25°C MIN	T_J = 25°C TYP (2)	T_J = 25°C MAX (3)	AT TEMPERATURE EXTREMES (1) MIN	AT TEMPERATURE EXTREMES (1) TYP (2)	AT TEMPERATURE EXTREMES (1) MAX (3)	UNIT
DC ELECTRICAL CHARACTERISTICS									
V_{OS}	Input offset voltage	LMC6482AI		0.11	0.75			1.35	mV
		LMC6482I		0.11	3			3.7	
		LMC6482M		0.11	3			3.8	
TCV_{OS}	Input offset voltage average drift			1					µV/°C
I_B	Input current	LMC6482AI		0.02				4	pA
		LMC6482I		0.02				4	
		LMC6482M		0.02				10	
I_{OS}	Input offset current	LMC6482AI		0.01				2	pA
		LMC6482I		0.01				2	
		LMC6482M		0.01				5	
C_{IN}	Common-mode input capacitance			3					pF
R_{IN}	Input resistance			10					TeraΩ

(1) See *Recommended Operating Conditions* for operating temperature ranges.
(2) Typical values represent the most likely parametric norm.
(3) All limits are specified by testing or statistical analysis.

Electrical Characteristics for V^+ = 5 V (continued)

unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS			T_J = 25°C MIN	T_J = 25°C TYP(2)	T_J = 25°C MAX(3)	AT TEMPERATURE EXTREMES(1) MIN	AT TEMPERATURE EXTREMES(1) TYP(2)	AT TEMPERATURE EXTREMES(1) MAX(3)	UNIT
CMRR	Common-mode rejection ratio	0 V ≤ V_{CM} ≤ 15 V, V^+ = 15 V		LMC6482AI	70	82		67			dB
				LMC6482I	65	82		62			
				LMC6482M	65	82		60			
		0 V ≤ V_{CM} ≤ 5 V, V^+ = 5 V		LMC6482AI	70	82		67			
				LMC6482I	65	82		62			
				LMC6482M	65	82		60			
+PSRR	Positive power supply rejection ratio	5 V ≤ V^+ ≤ 15 V, V^- = 0 V, V_O = 2.5 V		LMC6482AI	70	82		67			dB
				LMC6482I	65	82		62			
				LMC6482M	65	82		60			
−PSRR	Negative power supply rejection ratio	−5 V ≤ V^- ≤ −15 V, V^+ = 0 V, V_O = −2.5 V		LMC6482AI	70	82		67			dB
				LMC6482I	65	82		62			
				LMC6482M	65	82		60			
V_{CM}	Input common-mode voltage	V^+ = 5 V and 15 V, For CMRR ≥ 50 dB		LMC6482AI		V^- − 0.3	−0.25			0	V
				LMC6482I		V^- − 0.3	−0.25			0	
				LMC6482M		V^- − 0.3	−0.25			0	
				LMC6482AI	V^+ + 0.25	V^+ + 0.3		V^+			V
				LMC6482I	V^+ + 0.25	V^+ + 0.3		V^+			
				LMC6482M	V^+ + 0.25	V^+ + 0.3		V^+			
A_V	Large signal voltage gain	R_L = 2 kΩ(4)	Sourcing	LMC6482AI	140	666		84			V/mV
				LMC6482I	120	666		72			
				LMC6482M	120	666		60			
			Sinking	LMC6482AI	35	75		20			V/mV
				LMC6482I	35	75		20			
				LMC6482M	35	75		18			
		R_L = 600 Ω(4)	Sourcing	LMC6482AI	80	300		48			V/mV
				LMC6482I	50	300		30			
				LMC6482M	50	300		25			
			Sinking	LMC6482AI	20	35		13			V/mV
				LMC6482I	15	35		10			
				LMC6482M	15	35		8			

(4) V^+ = 15 V, V_{CM} = 7.5 V and R_L connected to 7.5 V. For sourcing tests, 7.5 V ≤ V_O ≤ 11.5 V. For sinking tests, 3.5 V ≤ V_O ≤ 7.5 V.

Electrical Characteristics for V^+ = 5 V (continued)

unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		T_J = 25°C			AT TEMPERATURE EXTREMES[1]			UNIT
				MIN	TYP[2]	MAX[3]	MIN	TYP[2]	MAX[3]	
V_O	Output swing	V^+ = 5 V R_L = 2 kΩ to $V^+/2$	LMC6482AI	4.8	4.9		4.7			V
			LMC6482I	4.8	4.9		4.7			
			LMC6482M	4.8	4.9		4.7			
			LMC6482AI		0.1	0.18			0.24	
			LMC6482I		0.1	0.18			0.24	
			LMC6482M		0.1	0.18			0.24	
		V^+ = 5 V R_L = 600 Ω to $V^+/2$	LMC6482AI	4.5	4.7		4.24			V
			LMC6482I	4.5	4.7		4.24			
			LMC6482M	4.5	4.7		4.24			
			LMC6482AI		0.3	0.5			0.65	
			LMC6482I		0.3	0.5			0.65	
			LMC6482M		0.3	0.5			0.65	
		V^+ = 15 V R_L = 2k Ω to $V^+/2$	LMC6482AI	14.4	14.7		14.2			V
			LMC6482I	14.4	14.7		14.2			
			LMC6482M	14.4	14.7		14.2			
			LMC6482AI		0.16	0.32			0.45	
			LMC6482I		0.16	0.32			0.45	
			LMC6482M		0.16	0.32			0.45	
		V^+ = 15 V R_L = 600 Ω to $V^+/2$	LMC6482AI	13.4	14.1		13			V
			LMC6482I	13.4	14.1		13			
			LMC6482M	13.4	14.1		13			
			LMC6482AI		0.5	1			1.3	
			LMC6482I		0.5	1			1.3	
			LMC6482M		0.5	1			1.3	
I_{SC}	Output short circuit current V^+ = 5 V	Sourcing, V_O = 0 V	LMC6482AI	16	20		12			mA
			LMC6482I	16	20		12			
			LMC6482M	16	20		10			
		Sinking, V_O = 5 V	LMC6482AI	11	15		9.5			mA
			LMC6482I	11	15		9.5			
			LMC6482M	11	15		8			
I_{SC}	Output short circuit current V^+ = 15 V	Sourcing, V_O = 0 V	LMC6482AI	28	30		22			mA
			LMC6482I	28	30		22			
			LMC6482M	28	30		20			
		Sinking, V_O = 12 V[5]	LMC6482AI	30	30		24			mA
			LMC6482I	30	30		24			
			LMC6482M	30	30		22			
I_S	Supply current	Both Amplifiers V^+ = +5 V, V_O = $V^+/2$	LMC6482AI		1	1.4			1.8	mA
			LMC6482I		1	1.4			1.8	
			LMC6482M		1	1.4			1.9	
		Both Amplifiers V^+ = 15 V, V_O = $V^+/2$	LMC6482AI		1.3	1.6			1.9	mA
			LMC6482I		1.3	1.6			1.9	
			LMC6482M		1.3	1.6			2	

(5) Do not short circuit output to V^+, when V^+ is greater than 13 V or reliability will be adversely affected.

Electrical Characteristics for V+ = 5 V (continued)

unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 5 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS	T_J = 25°C			AT TEMPERATURE EXTREMES(1)			UNIT
			MIN	TYP(2)	MAX(3)	MIN	TYP(2)	MAX(3)	
AC ELECTRICAL CHARACTERISTICS									
SR	Slew rate(6)	LMC6482AI	1	1.3		0.7			V/µs
		LMC6482I	0.9	1.3		0.63			
		LMC6482M	0.9	1.3		0.54			
GBW	Gain-bandwidth product	V^+ = 15 V		1.5					MHz
φ_m	Phase margin			50					Deg
G_m	Gain margin			15					dB
	Amp-to-amp isolation	See (7)		150					dB
e_n	Input-referred voltage noise	F = 1 kHz V_{cm} = 1 V		37					nV/√Hz
I_n	Input-referred current noise	F = 1 kHz		0.03					pA/√Hz
T.H.D.	Total harmonic distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 4.1 V_{PP}		0.01%					
		F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 8.5 V_{PP} V^+ = 10 V		0.01%					

(6) V + = 15V. Connected as voltage follower with 10-V step input. Number specified is the slower of either the positive or negative slew rates.
(7) Input referred, V^+ = 15 V and R_L = 100 kΩ connected to 7.5 V. Each amp excited in turn with 1 kHz to produce V_O = 12 V_{PP}.

6.6 Electrical Characteristics for V+ = 3 V

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 3 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		T_J = 25°C			AT TEMPERATURE EXTREMES(1)			UNIT
				MIN	TYP(2)	MAX(3)	MIN	TYP(2)	MAX(3)	
DC ELECTRICAL CHARACTERISTICS										
V_{OS}	Input offset voltage	LMC6482AI			0.9	2			2.7	mV
		LMC6482I			0.9	3			3.7	
		LMC6482M			0.9	3			3.8	
TCV_{OS}	Input offset voltage average drift				2					µV/°C
I_B	Input bias current				0.02					pA
I_{OS}	Input offset current				0.01					pA
CMRR	Common mode rejection ratio	0 V ≤ V_{CM} ≤ 3 V	LMC6482AI	64	74					dB
			LMC6482I	60	74					
			LMC6482M	60	74					

(1) See *Recommended Operating Conditions* for operating temperature ranges.
(2) Typical values represent the most likely parametric norm.
(3) All limits are specified by testing or statistical analysis.

Electrical Characteristics for V^+ = 3 V (continued)

Unless otherwise specified, all limits specified for T_J = 25°C, V^+ = 3 V, V^- = 0 V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ.

PARAMETER		TEST CONDITIONS		T_J = 25°C			AT TEMPERATURE EXTREMES (1)			UNIT
				MIN	TYP (2)	MAX (3)	MIN	TYP (2)	MAX (3)	
PSRR	Power supply rejection ratio	3 V ≤ V^+ ≤ 15 V, V^- = 0 V	LMC6482AI	68	80					dB
			LMC6482I	60	80					
			LMC6482M	60	80					
V_{CM}	Input common-mode voltage	For CMRR ≥ 50 dB	LMC6482AI		V^- −0.25	0				V
			LMC6482I		V^- −0.25	0				
			LMC6482M		V^- −0.25	0				
			LMC6482AI	V^+	V^+ + 0.25					V
			LMC6482I	V^+	V^+ + 0.25					
			LMC6482M	V^+	V^+ + 0.25					
V_O	Output swing	R_L = 2 kΩ to $V^+/2$			2.8					V
					0.2					
		R_L = 600 Ω to $V^+/2$	LMC6482AI	2.5	2.7					
			LMC6482I	2.5	2.7					
			LMC6482M	2.5	2.7					
			LMC6482AI		0.37	0.6				
			LMC6482I		0.37	0.6				
			LMC6482M		0.37	0.6				
I_S	Supply current	Both amplifiers	LMC6482AI		0.825	1.2			1.5	mA
			LMC6482I		0.825	1.2			1.5	
			LMC6482M		0.825	1.2			1.6	
AC ELECTRICAL CHARACTERISTICS										
SR	Slew rate	See (4)			0.9					V/µs
GBW	Gain-bandwidth product				1					MHz
T.H.D.	Total harmonic distortion	f = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 2 V_{PP}			0.01%					

(4) Connected as voltage follower with 2-V step input. Number specified is the slower of either the positive or negative slew rates.

6.7 Typical Characteristics

at V_S = 15 V, single supply, and T_A = 25°C (unless otherwise specified)

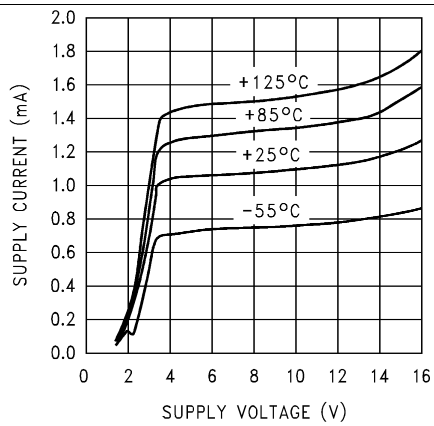


Figure 1. Supply Current vs Supply Voltage

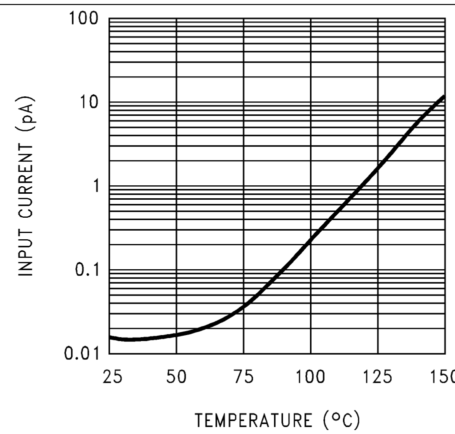


Figure 2. Input Current vs Temperature

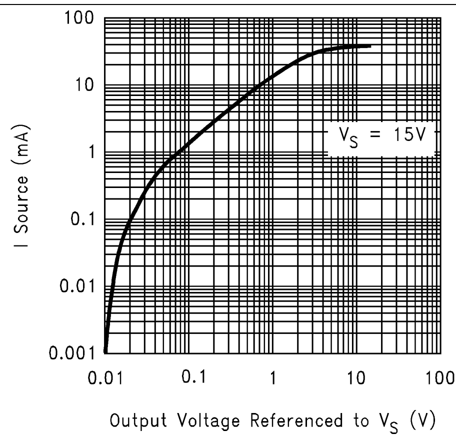


Figure 3. Sourcing Current vs Output Voltage

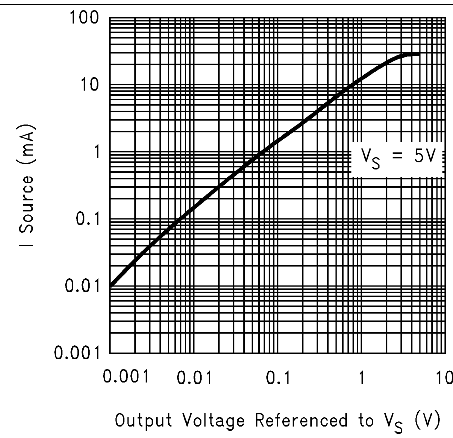


Figure 4. Sourcing Current vs Output Voltage

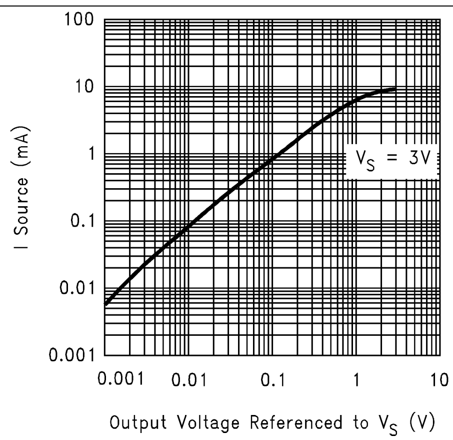


Figure 5. Sourcing Current vs Output Voltage

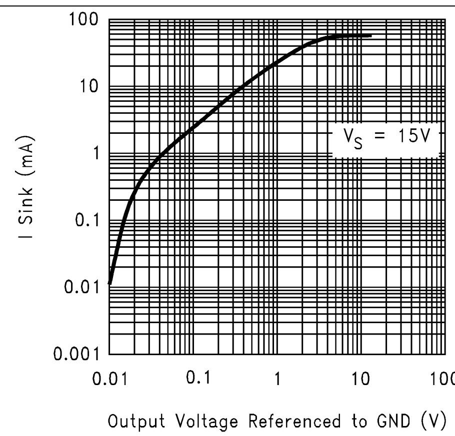


Figure 6. Sinking Current vs Output Voltage

Typical Characteristics (continued)

at V_S = 15 V, single supply, and T_A = 25°C (unless otherwise specified)

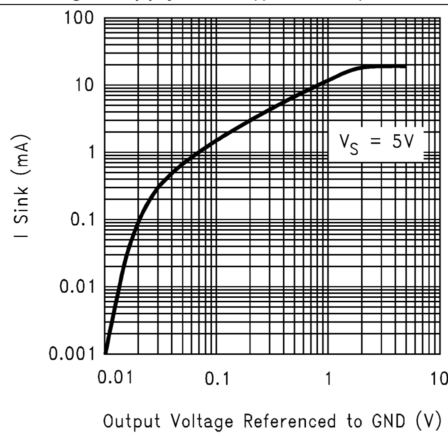


Figure 7. Sinking Current vs Output Voltage

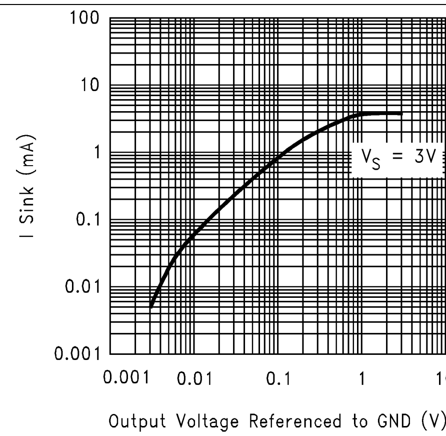


Figure 8. Sinking Current vs Output Voltage

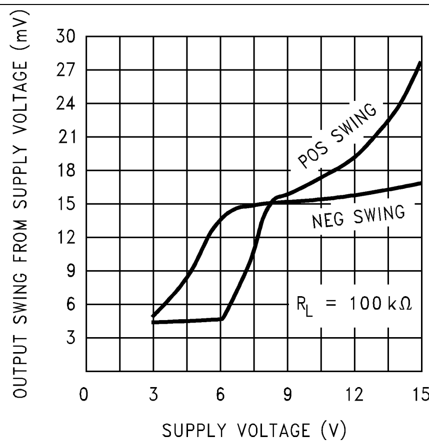


Figure 9. Output Voltage Swing vs Supply Voltage

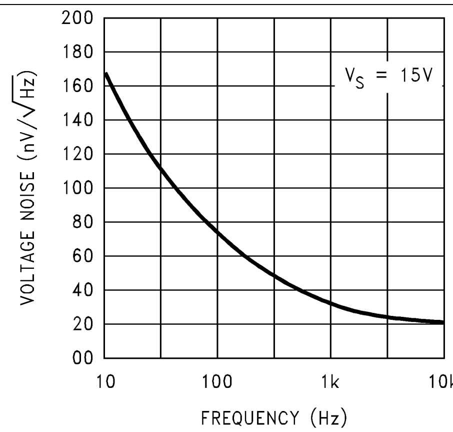


Figure 10. Input Voltage Noise vs Frequency

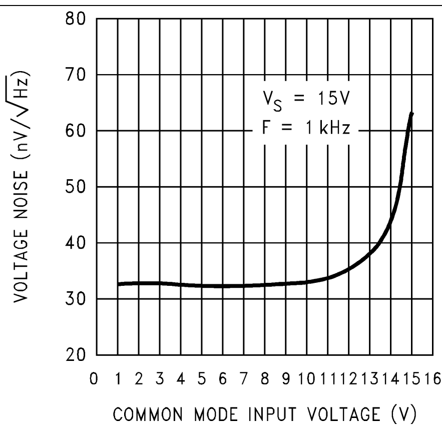


Figure 11. Input Voltage Noise vs Input Voltage

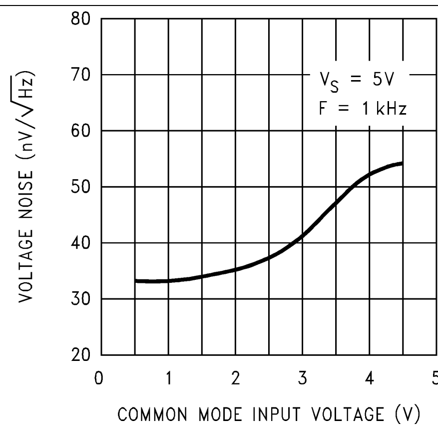


Figure 12. Input Voltage Noise vs Input Voltage

Typical Characteristics (continued)

at V_S = 15 V, single supply, and T_A = 25°C (unless otherwise specified)

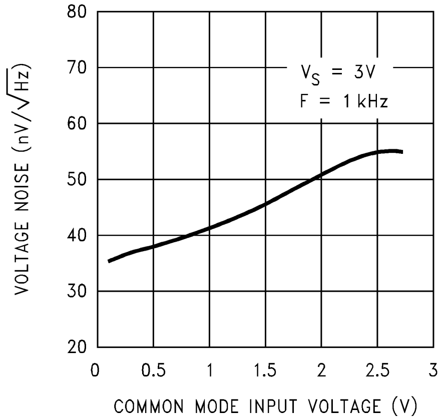


Figure 13. Input Voltage Noise vs Input Voltage

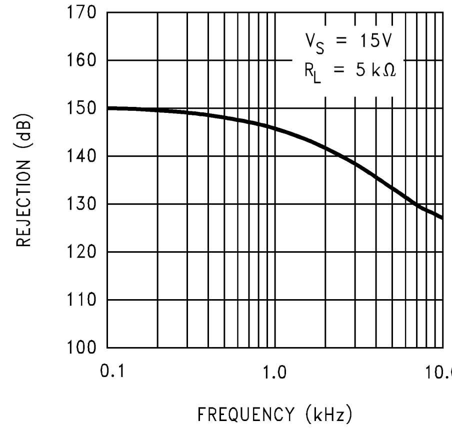


Figure 14. Crosstalk Rejection vs Frequency

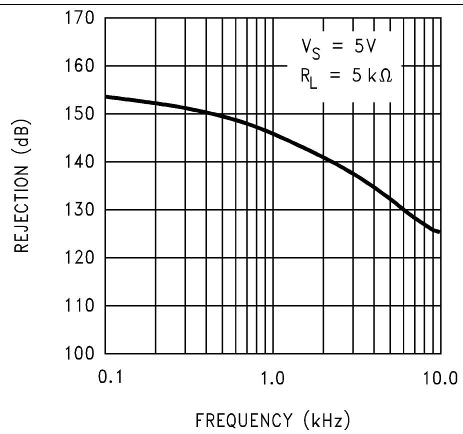


Figure 15. Crosstalk Rejection vs Frequency

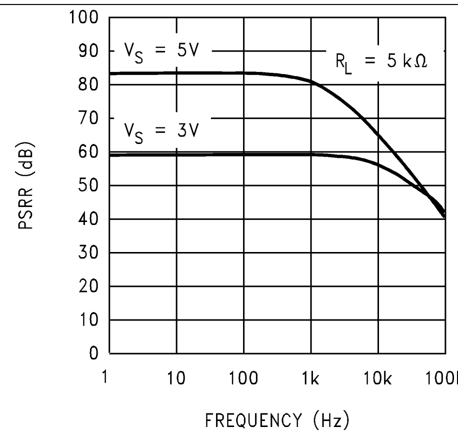


Figure 16. Positive PSRR vs Frequency

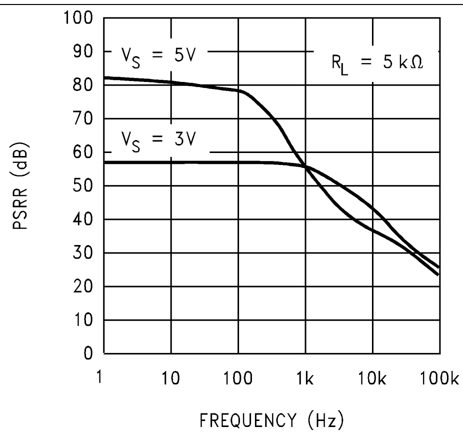


Figure 17. Negative PSRR vs Frequency

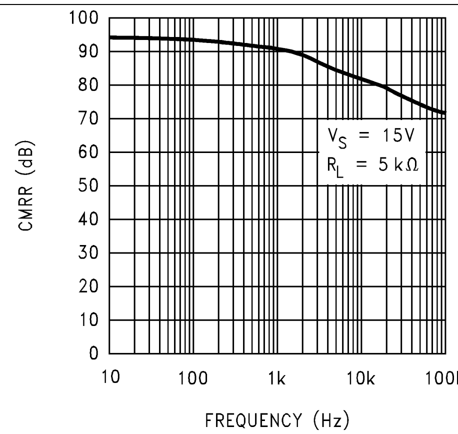


Figure 18. CMRR vs Frequency

Typical Characteristics (continued)

at V_S = 15 V, single supply, and T_A = 25°C (unless otherwise specified)

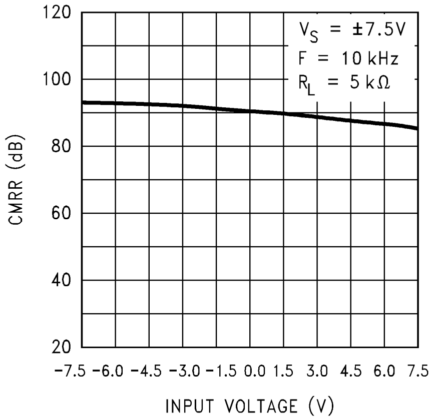


Figure 19. CMRR vs Input Voltage

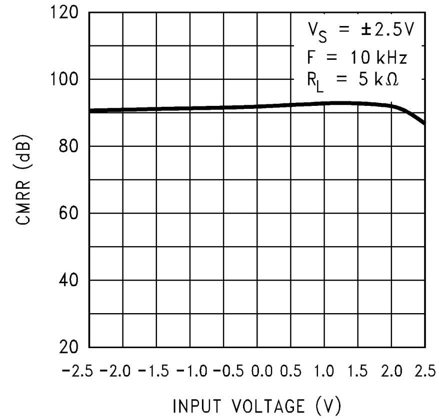


Figure 20. CMRR vs Input Voltage

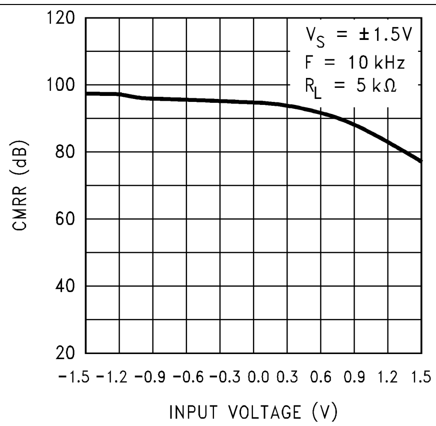


Figure 21. CMRR vs Input Voltage

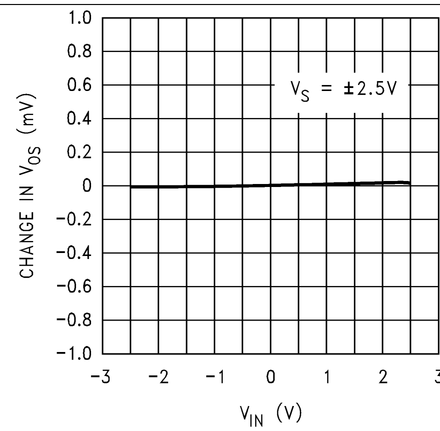


Figure 22. ΔV_{OS} vs CMR

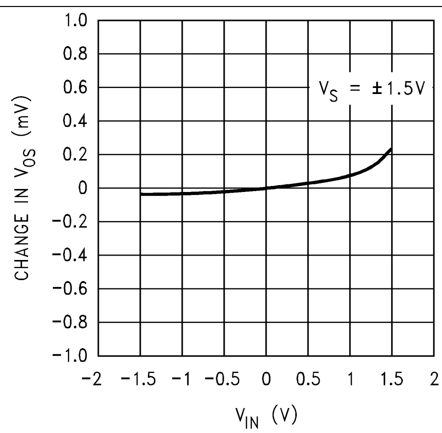


Figure 23. ΔV_{OS} vs CMR

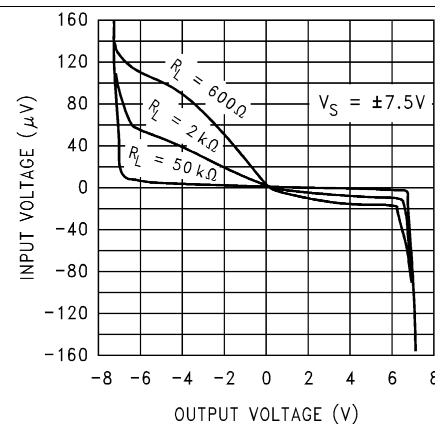


Figure 24. Input Voltage vs Output Voltage

Typical Characteristics (continued)

at V_S = 15 V, single supply, and T_A = 25°C (unless otherwise specified)

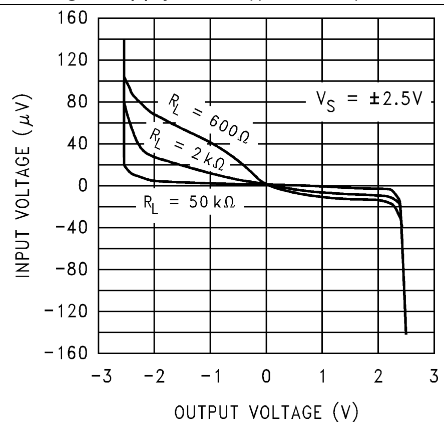


Figure 25. Input Voltage vs Output Voltage

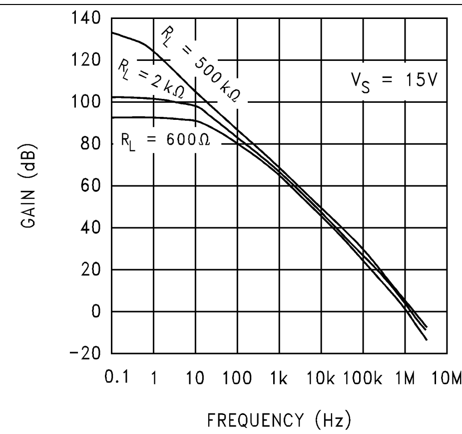


Figure 26. Open-Loop Frequency Response

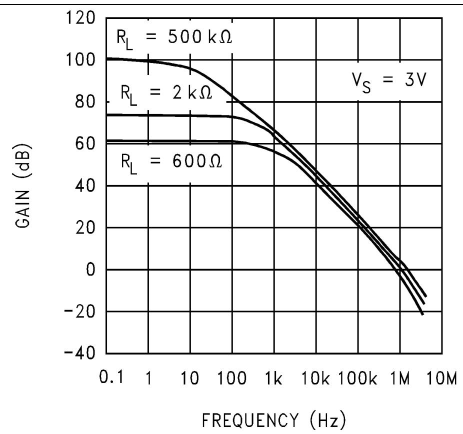


Figure 27. Open-Loop Frequency Response

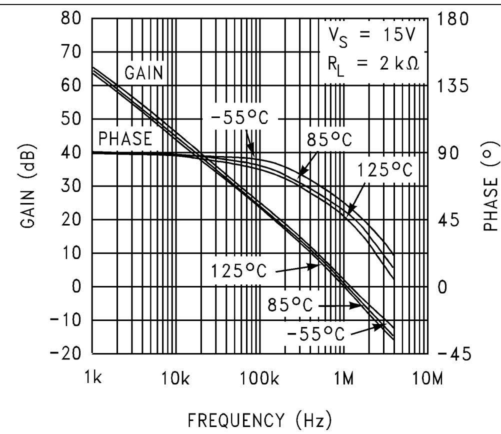


Figure 28. Open-Loop Frequency Response vs Temperature

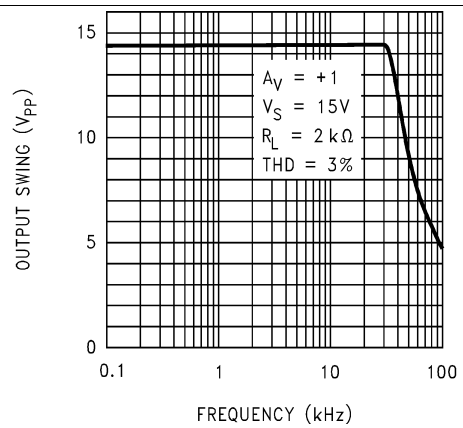


Figure 29. Maximum Output Swing vs Frequency

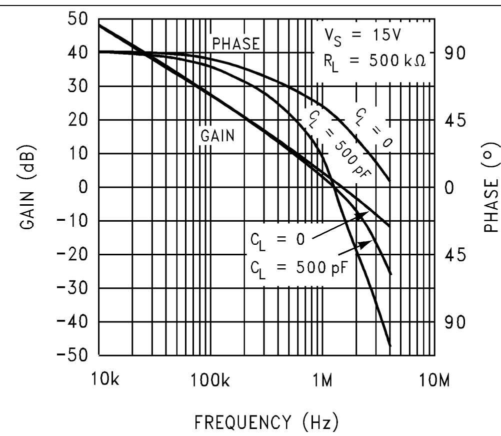


Figure 30. Gain and Phase vs Capacitive Load

Typical Characteristics (continued)

at V_S = 15 V, single supply, and T_A = 25°C (unless otherwise specified)

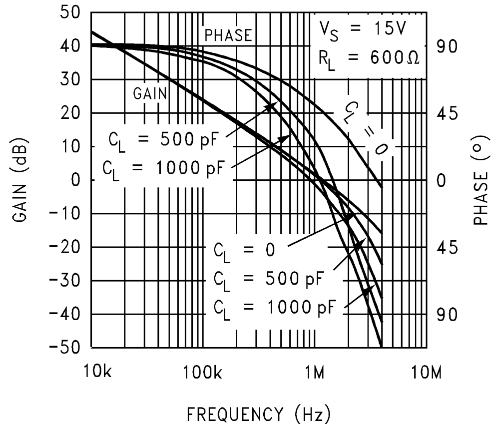


Figure 31. Gain and Phase vs Capacitive Load

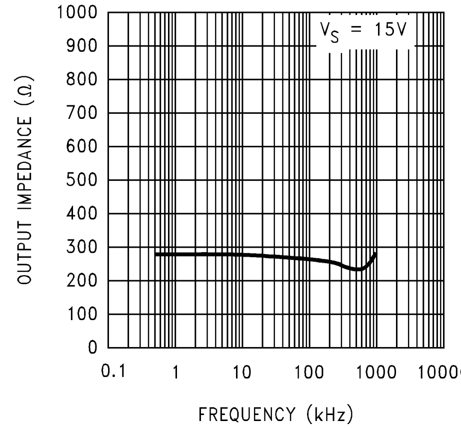


Figure 32. Open-Loop Output Impedance vs Frequency

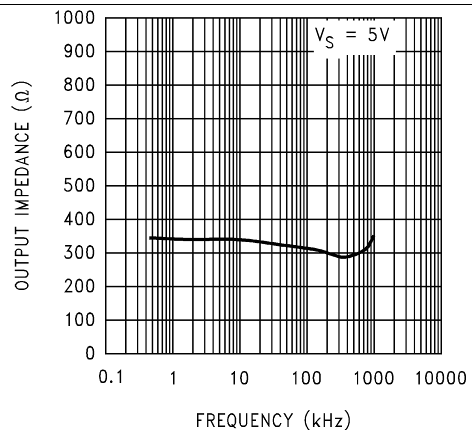


Figure 33. Open-Loop Output Impedance vs Frequency

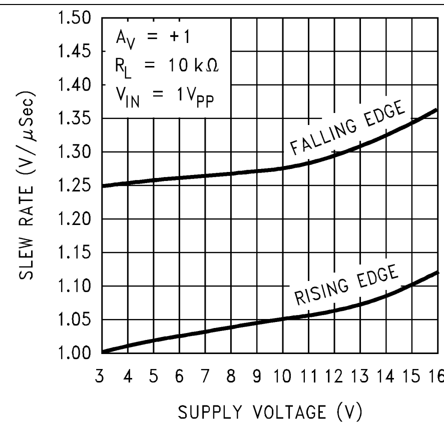


Figure 34. Slew Rate vs Supply Voltage

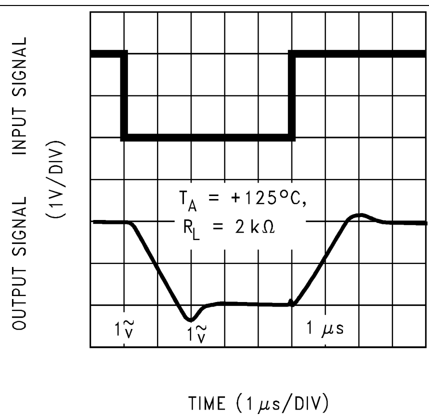


Figure 35. Noninverting Large Signal Pulse Response

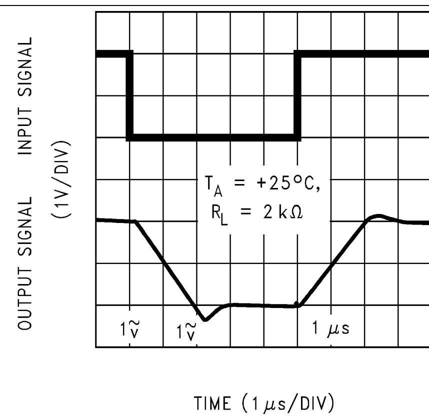


Figure 36. Noninverting Large Signal Pulse Response

Typical Characteristics (continued)

at V_S = 15 V, single supply, and T_A = 25°C (unless otherwise specified)

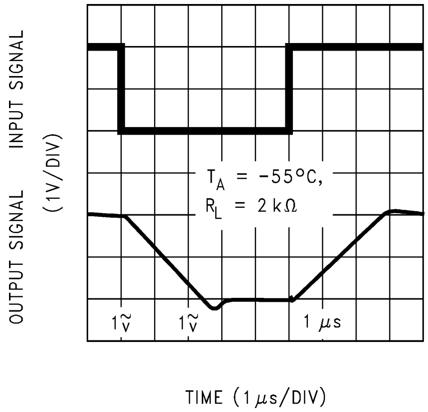


Figure 37. Noninverting Large Signal Pulse Response

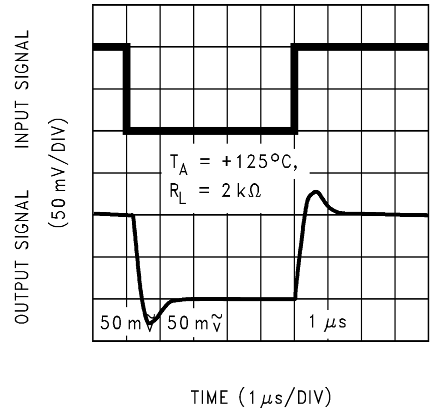


Figure 38. Noninverting Small Signal Pulse Response

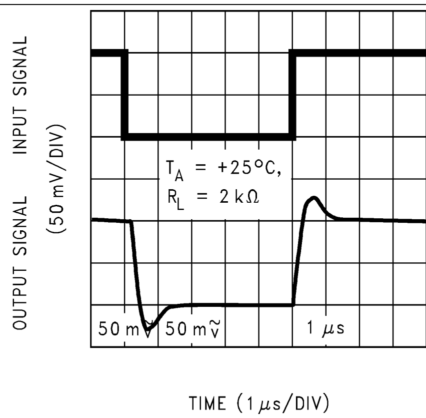


Figure 39. Noninverting Small Signal Pulse Response

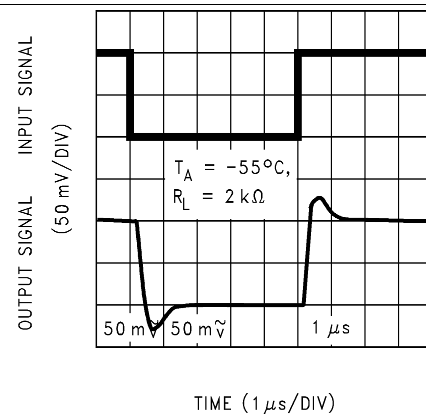


Figure 40. Noninverting Small Signal Pulse Response

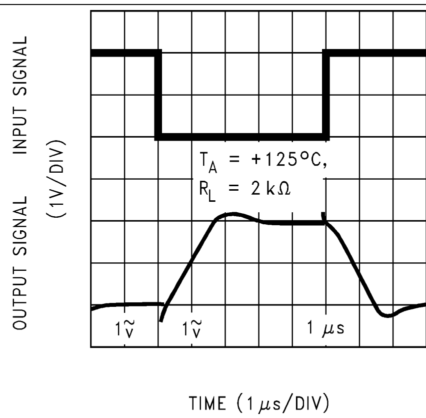


Figure 41. Inverting Large Signal Pulse Response

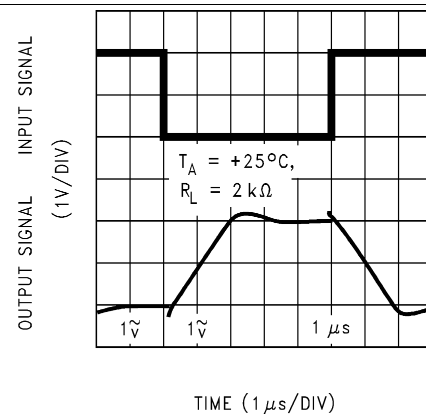


Figure 42. Inverting Large Signal Pulse Response

Typical Characteristics (continued)

at V_S = 15 V, single supply, and T_A = 25°C (unless otherwise specified)

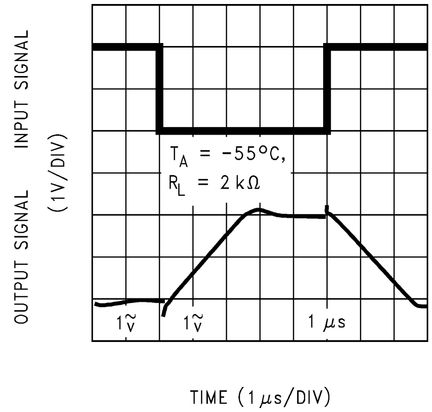


Figure 43. Inverting Large Signal Pulse Response

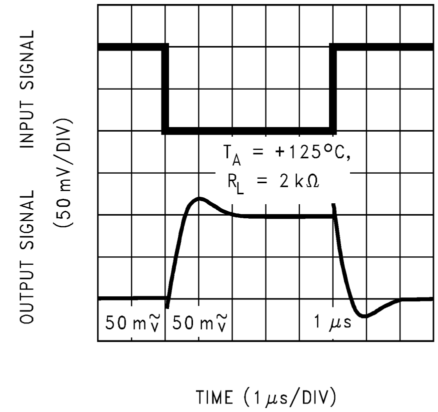


Figure 44. Inverting Small Signal Pulse Response

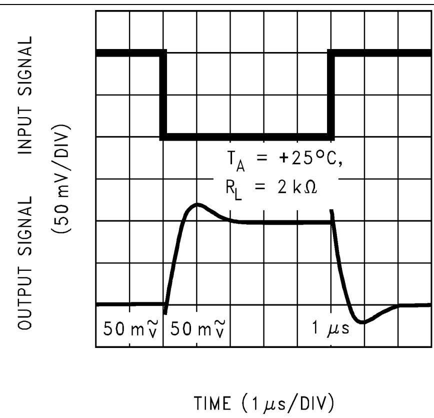


Figure 45. Inverting Small Signal Pulse Response

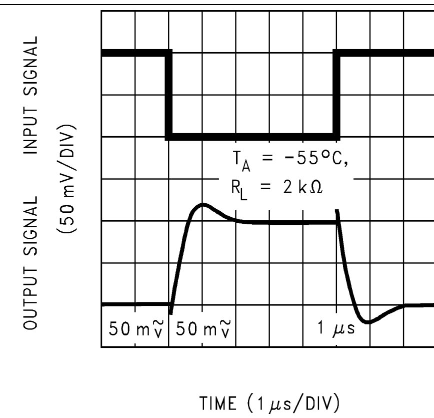


Figure 46. Inverting Small Signal Pulse Response

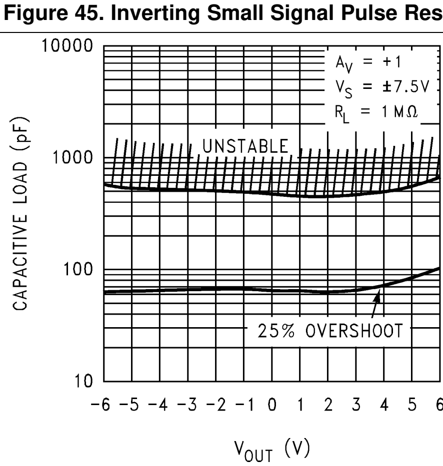


Figure 47. Stability vs Capacitive Load

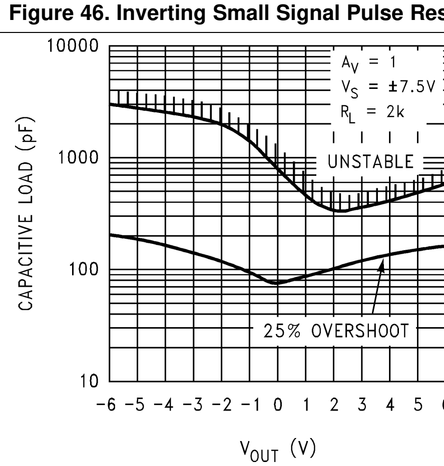


Figure 48. Stability vs Capacitive Load

Typical Characteristics (continued)

at V_S = 15 V, single supply, and T_A = 25°C (unless otherwise specified)

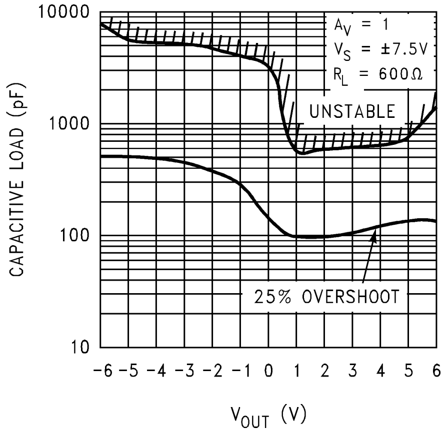


Figure 49. Stability vs Capacitive Load

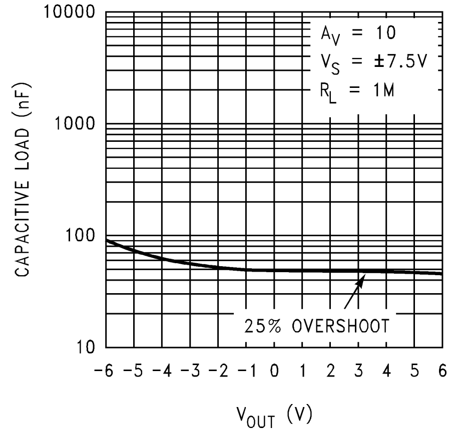


Figure 50. Stability vs Capacitive Load

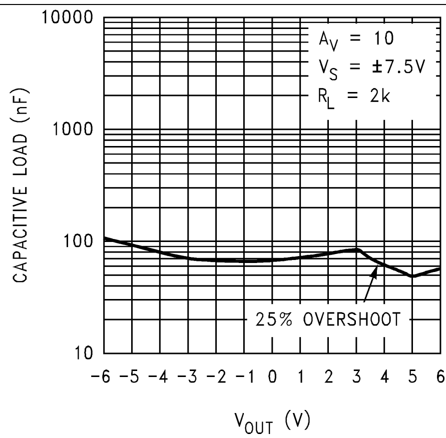


Figure 51. Stability vs Capacitive Load

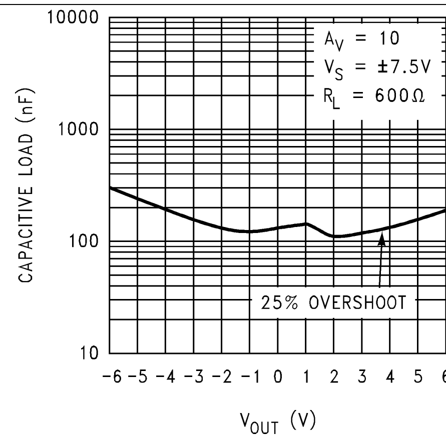


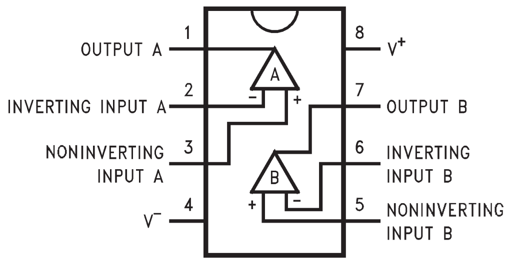
Figure 52. Stability vs Capacitive Load

7 Detailed Description

7.1 Overview

The LMC6482 is a dual CMOS operational amplifier that supports both rail-to-rail inputs and outputs. The device can be operated in both dual-supply mode and single-supply mode.

7.2 Functional Block Diagram



7.3 Feature Description

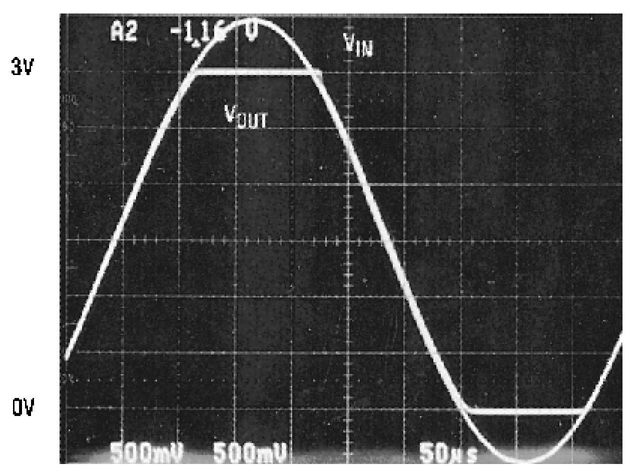
7.3.1 Amplifier Topology

The LMC6482 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common-mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, crossover distortion, and open-loop gain variation.

The LMC6482s input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

7.3.2 Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC6482 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 53 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

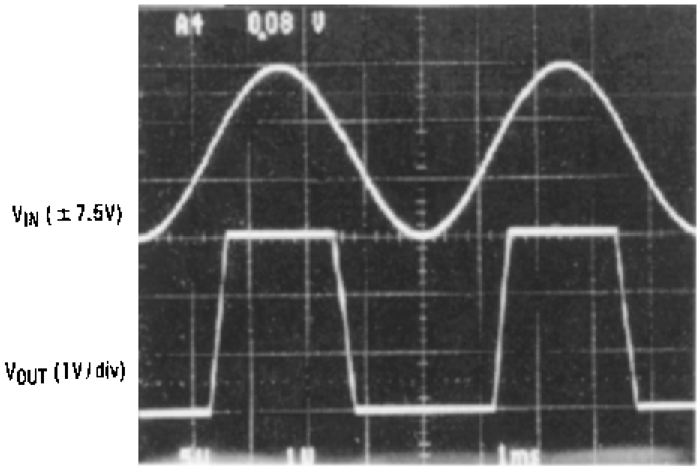


An input voltage signal exceeds the lMC6482 power supply voltages with no output phase inversion.

Figure 53. Input Voltage

Feature Description (continued)

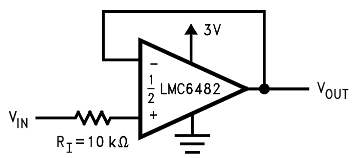
The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 54, can cause excessive current to flow in or out of the input pins possibly affecting reliability.



NOTE: A ±7.5-V input signal greatly exceeds the 3-V supply in Figure 55 causing no phase inversion due to R_I.

Figure 54. Input Signal

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor (R_I) as shown in Figure 55.



NOTE: R_I input current protection for voltages exceeding the supply voltages.

Figure 55. R_I Input Current Protection for Voltages Exceeding the Supply Voltages

7.3.3 Rail-to-Rail Output

The approximated output resistance of the LMC6482 is 180-Ω sourcing and 13-0Ω sinking at V_S = 3 V and 110-Ω sourcing and 80-Ω sinking at V_S = 5 V. Using the calculated output resistance, the maximum output voltage swing can be estimated as a function of load.

7.4 Device Functional Modes

The LMC6482 can be used in applications where each amplifier channel is used independently, or in applications in which the channels are cascaded. See the *Typical Applications* section for more information.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

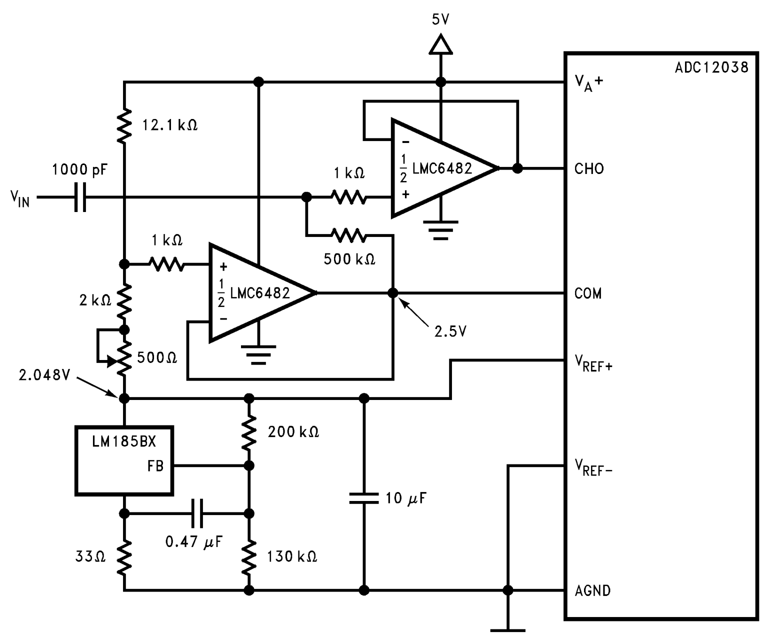
8.1.1 Upgrading Applications

The LMC6484 quads and LMC6482 duals have industry-standard pin outs to retrofit existing applications. System performance can be greatly increased by the features of the LMC6482. The key benefit of designing in the LMC6482 is increased linear signal range. Most op-amps have limited input common-mode ranges. Signals that exceed this range generate a nonlinear output response that persists long after the input signal returns to the common-mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common-mode ranges resulting in output phase inversion or severe distortion.

8.1.2 Data Acquisition Systems

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6482 (Figure 56). Capable of using the full supply range, the LMC6482 does not require input signals to be scaled down to meet limited common-mode voltage ranges. The LMC4282 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to ±0.325 LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.



NOTE: Operating from the same supply voltage, the LMC6482 buffers the ADC12038 maintaining excellent accuracy.

Figure 56. Buffering the ADC12038 With the LMC6482

Application Information (continued)

8.1.3 Instrumentation Circuits

The LMC6482 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6482 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6482 an excellent choice of noisy or industrial environments. Other applications that benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with R_g to set the differential gain of the 3-op-amp instrumentation circuit in Figure 57. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

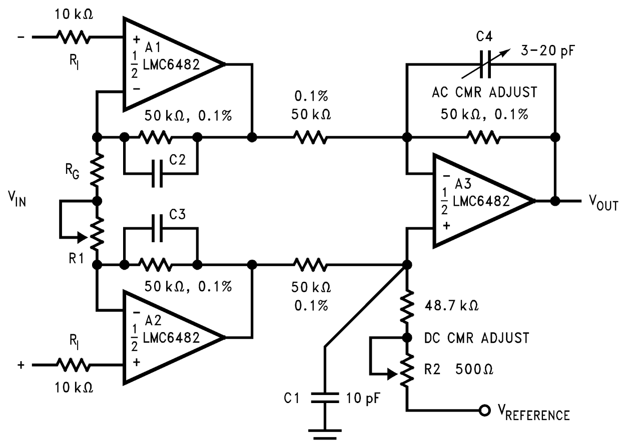


Figure 57. Low-Power, Three-Op-Amp Instrumentation Amplifier

A two-op-amp instrumentation amplifier designed for a gain of 100 is shown in Figure 58. Low sensitivity trimming is made for offset voltage, CMRR, and gain. Low cost and low power consumption are the main advantages of this two-op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three-op-amp instrumentation amplifier.

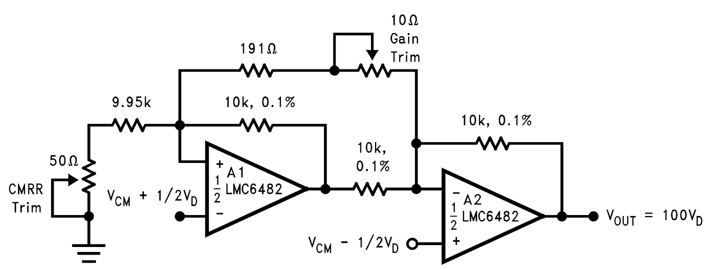


Figure 58. Low-Power, Two-Op-Amp Instrumentation Amplifier

8.1.4 Spice Macromodel

A spice macromodel is available for the LMC6482. This model includes accurate simulation of the following:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

Many more characteristics are listed on the macromodel disk.

Contact your local TI sales office to obtain an operational amplifier spice model library disk.

8.2 Typical Applications

8.2.1 3-V Single-Supply Buffer Circuit

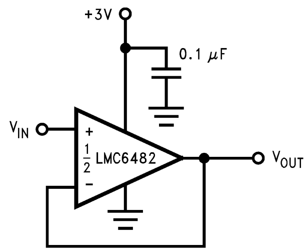


Figure 59. 3-V Single-Supply Buffer Circuit

8.2.1.1 Design Requirements

For best performance, make sure that the input voltage swing is between V+ and V–.

Also, make certain that the input does not exceed the common-mode input range.

To reduce the risk of destabilizing the output, use resistive isolation on the output when driving capacitive loads (see the *Detailed Design Procedure* section).

When large feedback resistors are used, compensation for parasitic capacitance on the input may be necessary. See the *Detailed Design Procedure* section.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Capacitive Load Compensation

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 60. This simple technique is useful for isolating the capacitive inputs of multiplexers and A/D converters.

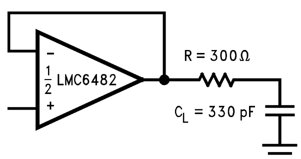


Figure 60. Resistive Isolation of a 330-pF Capacitive Load

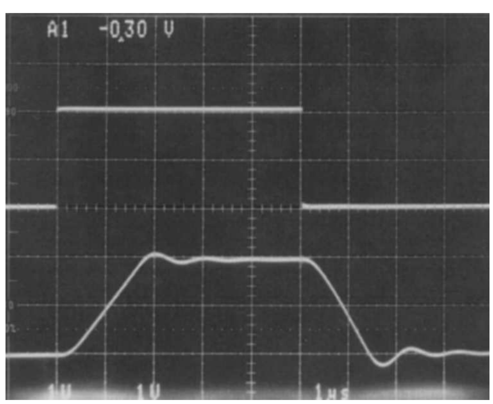


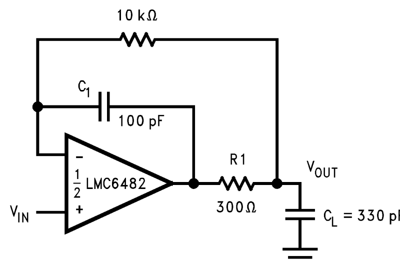
Figure 61. Pulse Response of the LMC6482 Circuit in Figure 60

Typical Applications (continued)

8.2.1.2.2 Capacitive Load Tolerance

The LMC6482 can typically directly drive a 100-pF load with V_S = 15 V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the output impedance of the op-amp and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Improved frequency response is achieved by indirectly driving capacitive loads, as shown in Figure 62.



NOTE: Compensated to handle a 330-pF capacitive load.

Figure 62. LMC6482 Noninverting Amplifier

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high-frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response is shown in Figure 63.

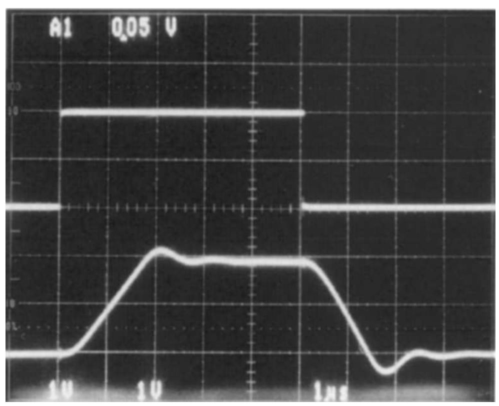


Figure 63. Pulse Response of Lmc6482 Circuit in Figure 62

8.2.1.2.3 Compensating For Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6482. Large feedback resistors can react with small values of input capacitance due to transducers, photo diodes, and circuits board parasitics to reduce phase margins.

Typical Applications (continued)

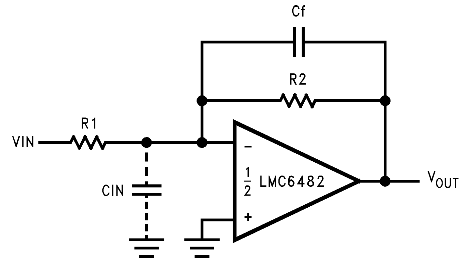


Figure 64. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 64), C_f, is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \tag{1}$$

or

$$R_1 C_{IN} \leq R_2 C_f \tag{2}$$

which typically provides significant overcompensation.

Printed-circuit-board stray capacitance may be larger or smaller than that of a bread-board, so the actual optimum value for C_f may be different. The values of C_f should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

8.2.1.2.4 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in Figure 65 and Figure 66. Large value resistances and potentiometers are used to reduce power consumption while providing typically ±2.5 mV of adjustment range, referred to the input, for both configurations with V_S = ±5 V.

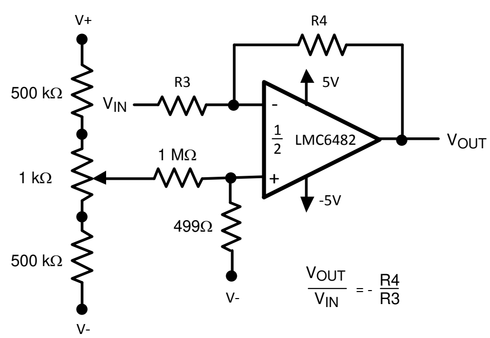


Figure 65. Inverting Configuration Offset Voltage Adjustment

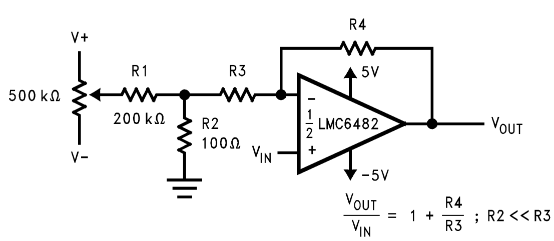


Figure 66. Noninverting Configuration Offset Voltage Adjustment

Typical Applications (continued)

8.2.1.3 Application Curves

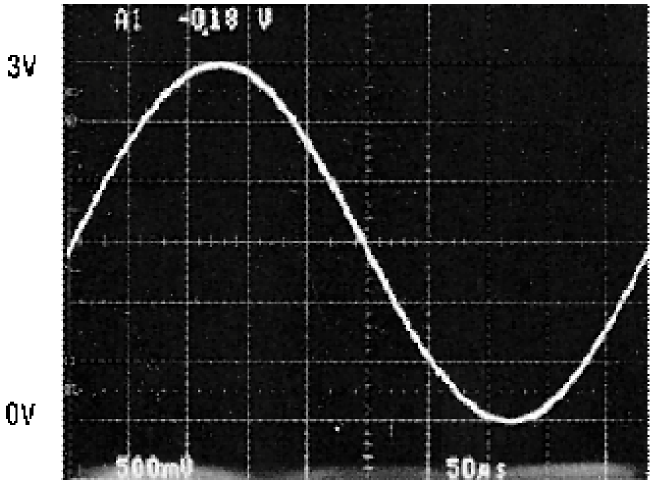


Figure 67. Rail-To-Rail Input

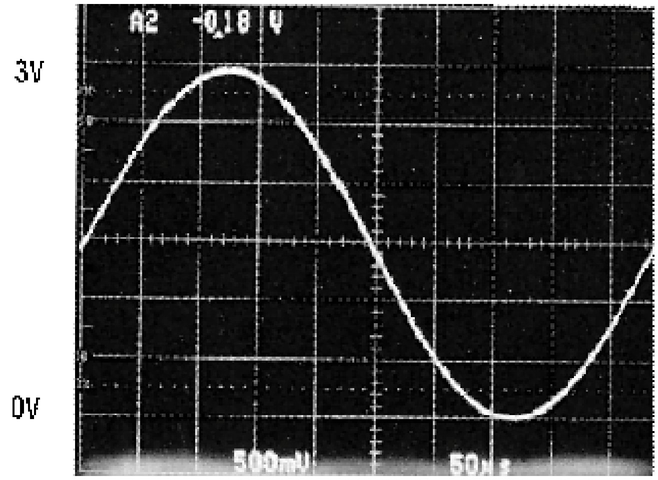


Figure 68. Rail-To-Rail Output

8.2.2 Typical Single-Supply Applications

The circuit in Figure 69 uses a single supply to half-wave rectify a sinusoid centered about ground. R_I limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full-wave rectification is provided by the circuit in Figure 71.

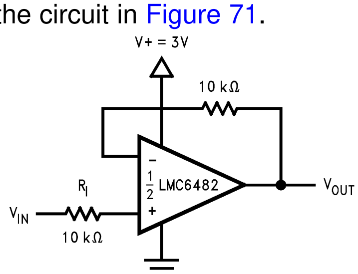


Figure 69. Half-Wave Rectifier With Input Current Protection (R_I)

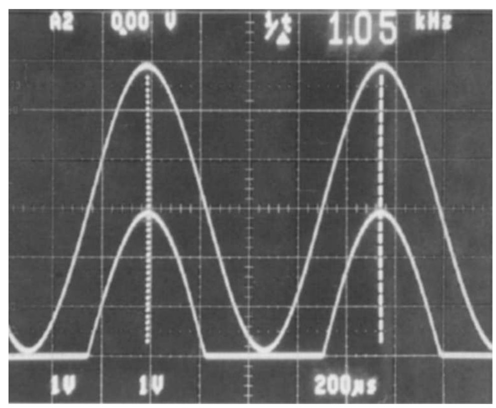


Figure 70. Half-Wave Rectifier Waveform

Typical Applications (continued)

In Figure 75 dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. The ultra-low input current of the LMC6482 has a negligible effect on droop.

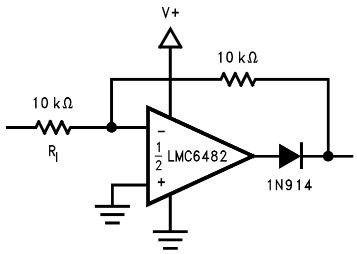


Figure 71. Full-Wave Rectifier With Input Current Protection (R_I)

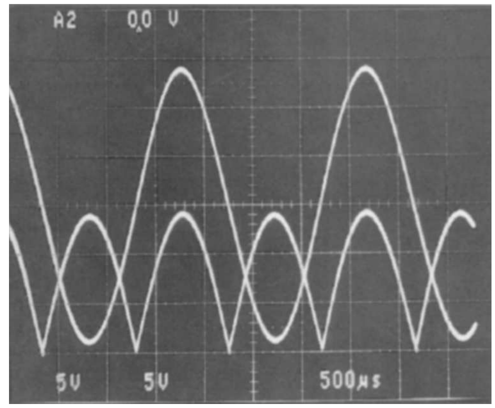


Figure 72. Full-Wave Rectifier Waveform

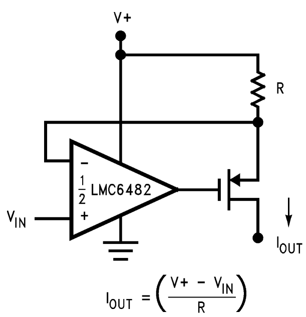


Figure 73. Large Compliance Range Current Source

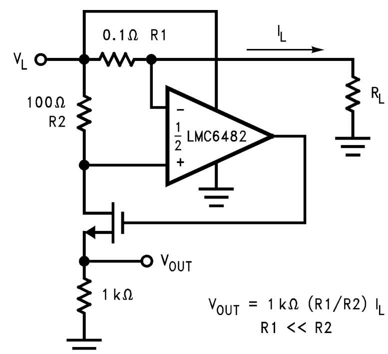


Figure 74. Positive Supply Current Sense

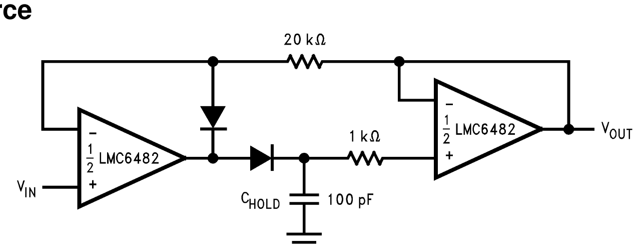


Figure 75. Low-Voltage Peak Detector With Rail-To-Rail Peak Capture Range

Typical Applications (continued)

The high CMRR (82 dB) of the LMC6482 allows excellent accuracy throughout the rail-to-rail dynamic capture range of the circuit.

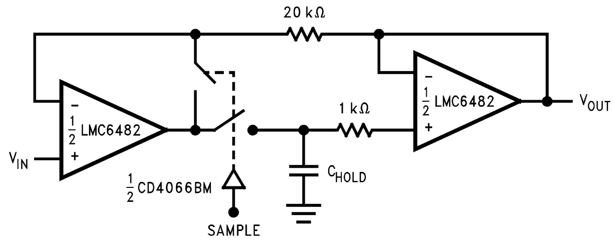
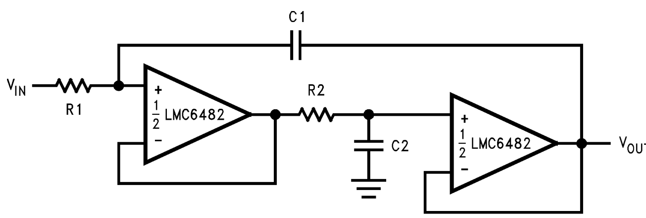


Figure 76. Rail-To-Rail Sample and Hold

The low-pass filter circuit in Figure 77 can be used as an antialiasing filter with the same voltage supply as the A/D converter.

Filter designs can also take advantage of the LMC6482 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors that take less board space and cost less.



$$R1 = R2, C1 = C2; f = \frac{1}{2\pi R1\ C1}; DF = ½ \sqrt{\frac{C_2}{C_1}} \sqrt{\frac{R_2}{R_1}}$$

Figure 77. Rail-To-Rail Single Supply Low Pass Filter

9 Power Supply Recommendations

The LMC6482 can be operated over a supply range of 3 V to 15 V. To achieve noise immunity as appropriate to the application, make sure to use good PCB layout practices for power supply rails and planes, as well as using bypass capacitors connected between the power supply pins and ground.

10 Layout

10.1 Layout Guidelines

It is generally recognized that any circuit that must operate with less than 1000 pA of leakage current requires special layout of the PC board. To take advantage of the ultra-low input current of the LMC6482, typically less than 20 fA, an excellent layout is essential. Fortunately, the techniques of obtaining low leakages are quite simple. First, do not ignore the surface leakage of the PCB, Even through the leakage current may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LM6482s inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, and so forth connected to the inputs of the op amp, as in Figure 78. To have a significant effect, place guard rings on both the top and bottom of the PCB. This PC foil must then be connected to a voltage that is at the same voltage as the amplifier inputs, because no leakage current can flow between two points at the same potential. For example, a PCB trace-to-pad resistance of 10^{12} Ω, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5-V bus adjacent to the pad of the input. This leakage would cause a 250 times degradation from the actual performance of the LMC6482. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11} Ω causes only 0.05 pA of leakage current. See Figure 79 through Figure 81 for typical connections of guard rings for standard op-amp configurations.

Be aware that when it is inappropriate to lay out a PCB for the sake of just a few circuits, another technique is even better than a guard ring on a PCB: Do not insert the input pin of the amplifier into the PCB at all, but bend it up in the air, and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PCB construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 82.

10.2 Layout Example

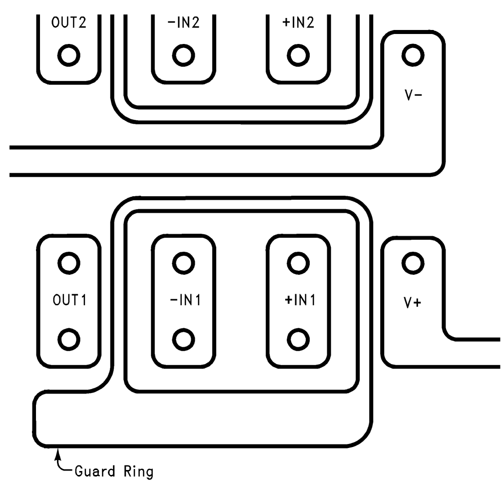


Figure 78. Example of Guard Ring in PCB Layout Typical Connections of Guard Rings

Layout Example (continued)

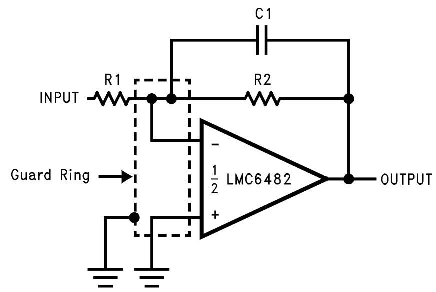


Figure 79. Inverting Amplifier Typical Connections of Guard Rings

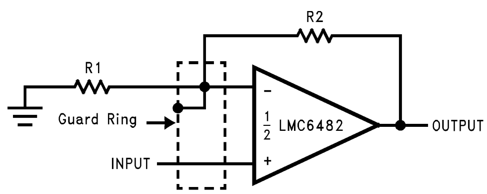


Figure 80. Noninverting Amplifier Typical Connections of Guard Rings

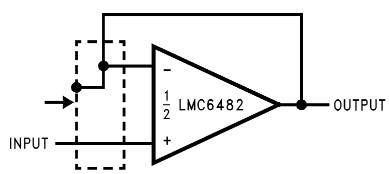
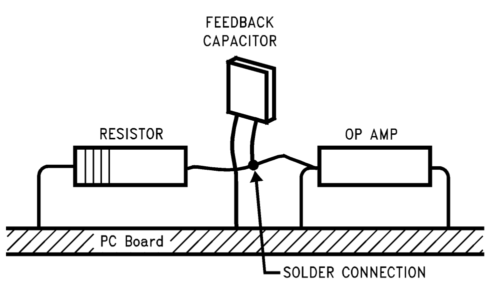


Figure 81. Follower Typical Connections of Guard Rings



NOTE: Input pins are lifted out of PCB and soldered directly to components. All other pins connected to PCB.

Figure 82. Air Wiring

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC6482AIM	NRND	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LMC64 82AIM	
LMC6482AIM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 82AIM	Samples
LMC6482AIMX	NRND	SOIC	D	8	2500	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LMC64 82AIM	
LMC6482AIMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 82AIM	Samples
LMC6482AIN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	Call TI | SN	Level-1-NA-UNLIM	-40 to 85	LMC64 82AIN	Samples
LMC6482IM	NRND	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LMC64 82IM	
LMC6482IM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 82IM	Samples
LMC6482IMM	NRND	VSSOP	DGK	8	1000	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	A10	
LMC6482IMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A10	Samples
LMC6482IMMX	NRND	VSSOP	DGK	8	3500	Non-RoHS & Green	Call TI	Level-1-260C-UNLIM	-40 to 85	A10	
LMC6482IMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	A10	Samples
LMC6482IMX	NRND	SOIC	D	8	2500	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LMC64 82IM	
LMC6482IMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC64 82IM	Samples
LMC6482IN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	Call TI	Level-1-NA-UNLIM	-40 to 85	LMC6482IN	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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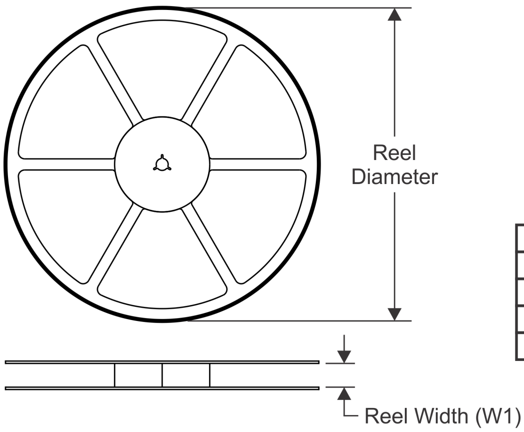
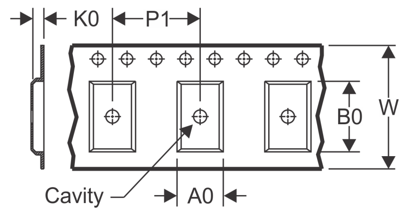
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

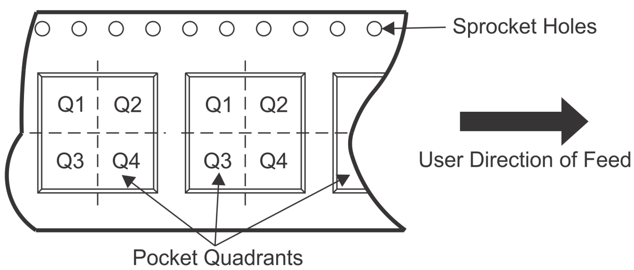
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

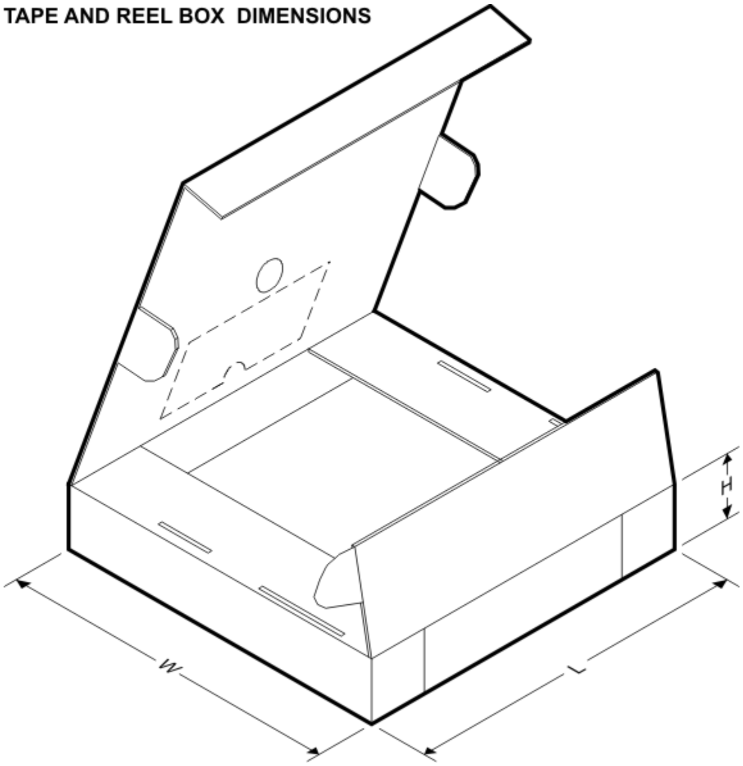
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC6482AIMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6482AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6482IMM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC6482IMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC6482IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

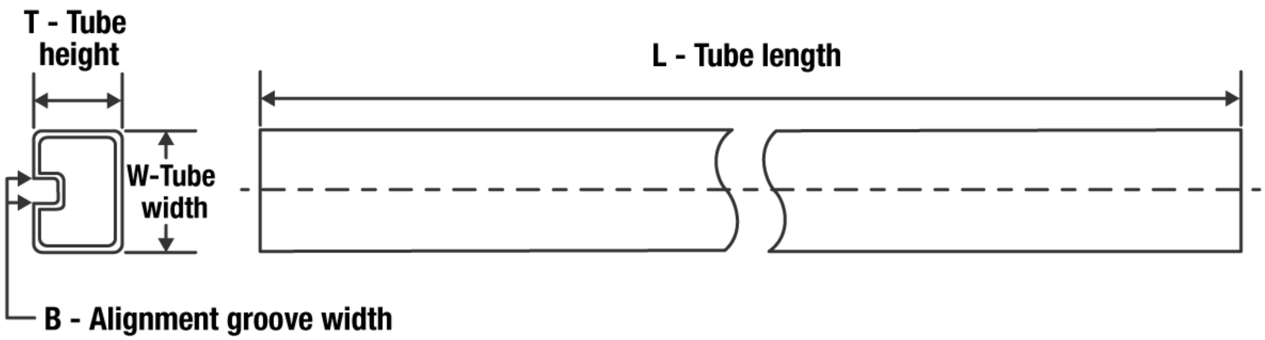
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

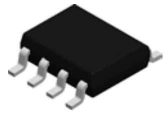
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC6482AIMX	SOIC	D	8	2500	367.0	367.0	35.0
LMC6482AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC6482IMM	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMC6482IMM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMC6482IMMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC6482IMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC6482IMX	SOIC	D	8	2500	367.0	367.0	35.0
LMC6482IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

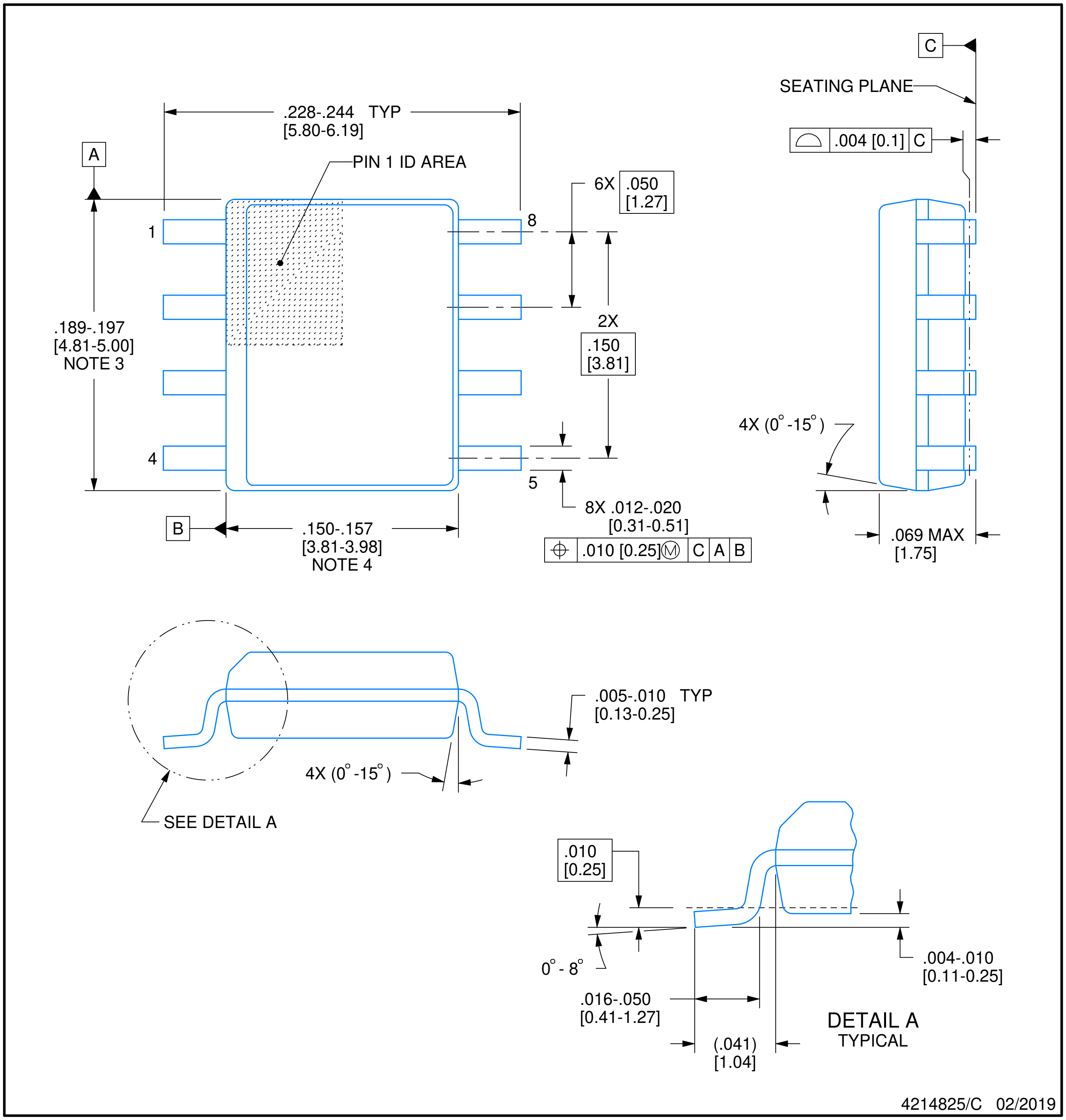
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMC6482AIM	D	SOIC	8	95	495	8	4064	3.05
LMC6482AIM	D	SOIC	8	95	495	8	4064	3.05
LMC6482AIM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMC6482AIN/NOPB	P	PDIP	8	40	502	14	11938	4.32
LMC6482IM	D	SOIC	8	95	495	8	4064	3.05
LMC6482IM	D	SOIC	8	95	495	8	4064	3.05
LMC6482IM/NOPB	D	SOIC	8	95	495	8	4064	3.05
LMC6482IN/NOPB	P	PDIP	8	40	502	14	11938	4.32



PACKAGE OUTLINE

SOIC - 1.75 mm max height

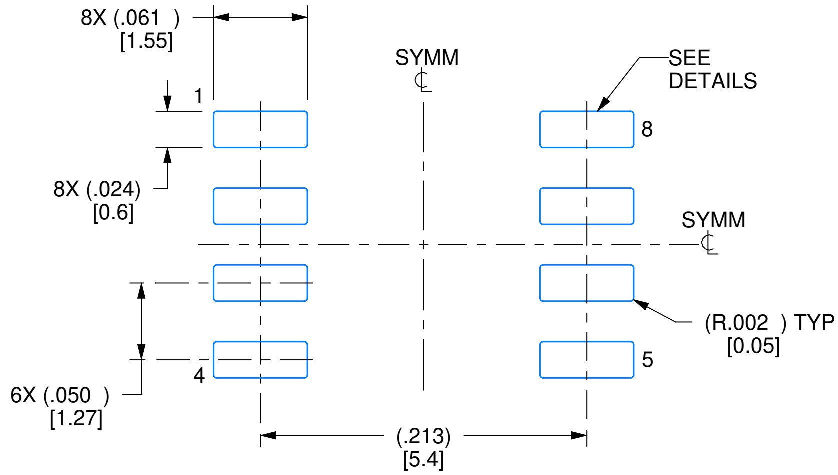
SMALL OUTLINE INTEGRATED CIRCUIT



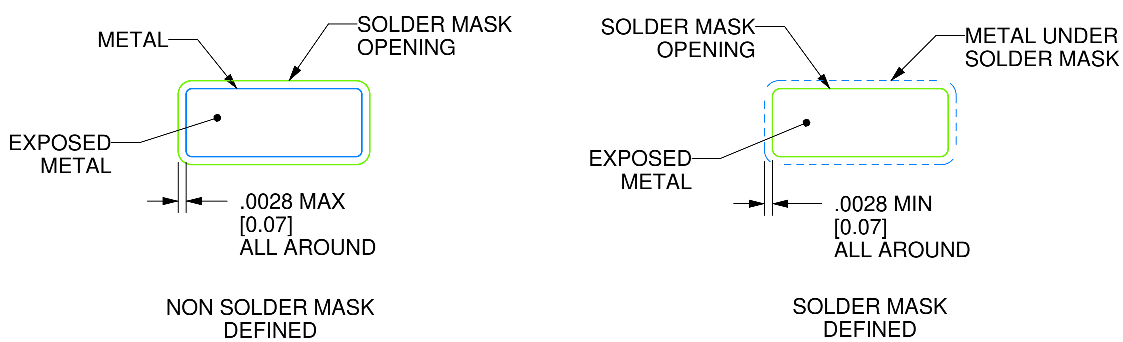
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

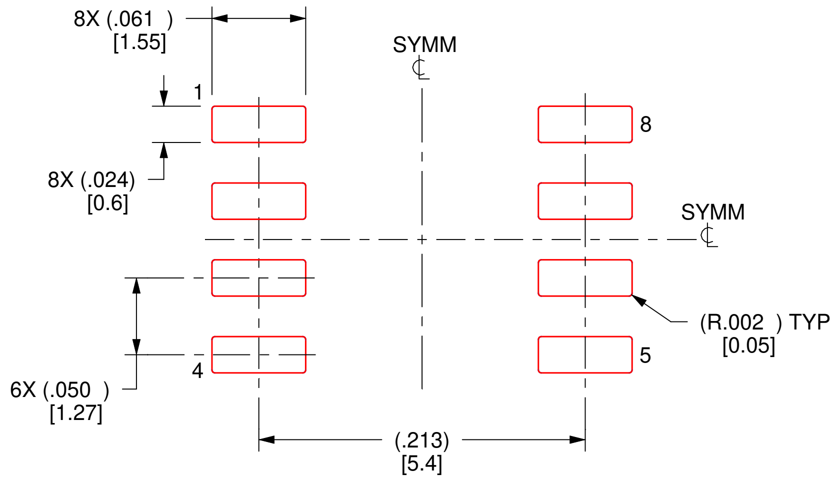


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



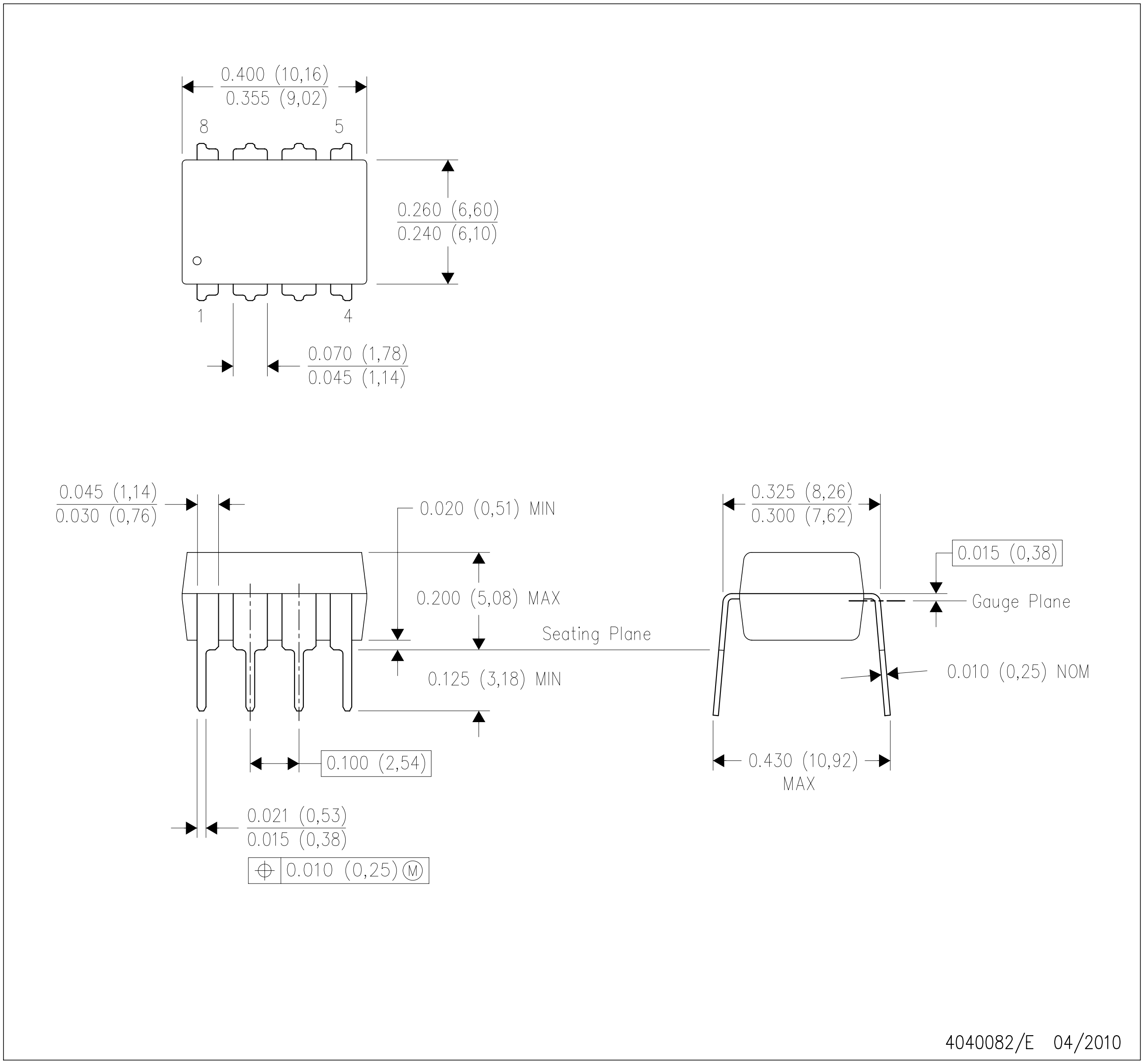
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

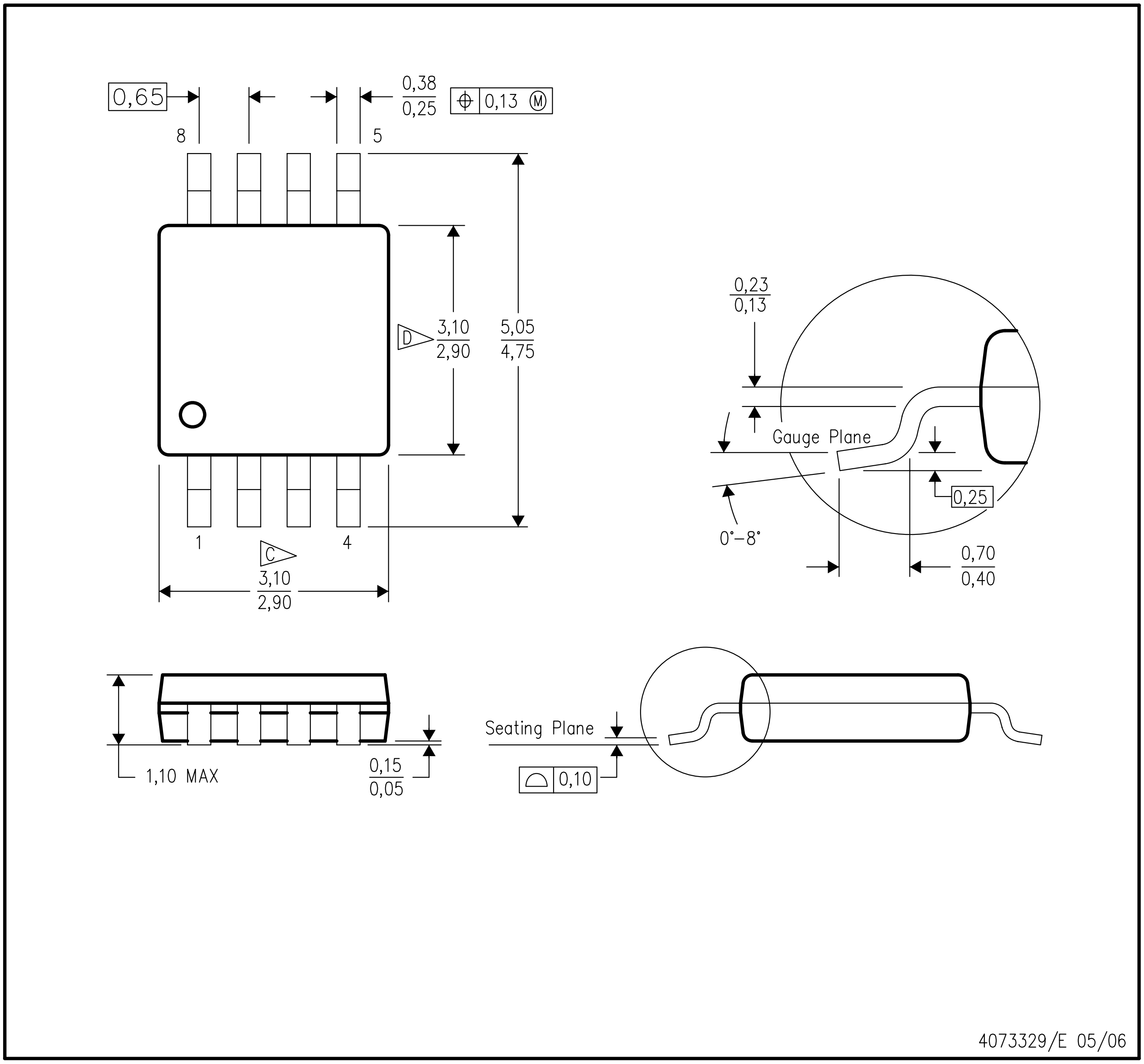
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



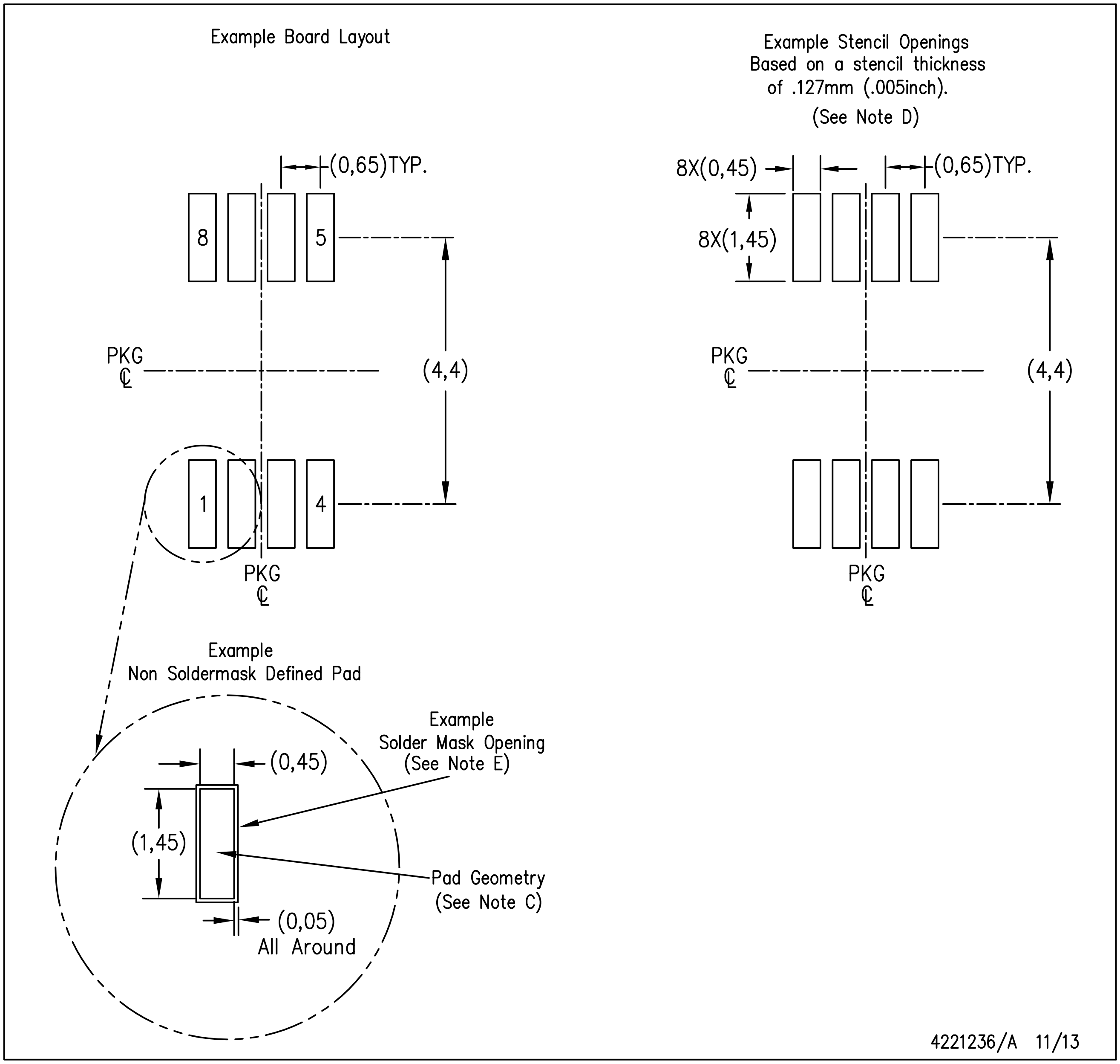
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.