CYPRESS SEMICONDUCTOR

64 x 4 FIFO Serial Memory

Features

- **1.2-/2-MHz data rate**
- **Fully TTL compatible**
- **Independent asynchronous inputs and outputs**
- **Direct replacement for PMOS 3341**
- **Expandable in word length and width**
- **CMOS for optimum speed/power**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The 3341 is a 64-word x 4-bit first-in first-out (FIFO) serial memory. The inputs and outputs are completely independent (no common clocks), making the 3341 ideal for asynchronous buffer applications.

Control signals are provided for both vertical and horizontal expansion.

The 3341 is manufactured using a Cypress CMOS technology and is available in both ceramic and plastic packages.

Data Input

The four bits of data on the D_0 through D_3 inputs are entered into the first location when both input ready (IR) and shift in (SI) are HIGH. This causes IR to go LOW, but data will stay locked in the first bit location until both IR and SI are LOW. Then data will propagate to the second bit location, provided the location is empty. When data is transferred, IR will go HIGH, indicating that the device is ready to accept new data. If the memory is full, IR will stay LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus, data will stack up at the end of the device while empty locations will "bubble" to the front. t_{BT} defines the time required for the first data to travel from the input to the output of a previously empty device, or for the first empty space to travel from the output to the input of a previously full device.

Data Output

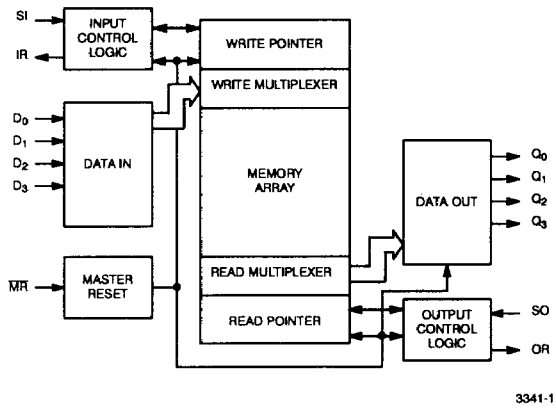
When data has been transferred into the last cell, output ready (OR) goes HIGH, indicating the presence of valid data at the output pins Q_0 through Q_3. The transfer of data is initiated when both the OR output from the device and the shift out (SO) input to the device are HIGH. This causes OR to go LOW; output data, however, is maintained until both OR and SO are LOW. Then the content of the adjacent (upstream) cell (provided it is full) will be transferred into the last cell, causing OR to go HIGH again. If the memory has been emptied, OR will stay LOW.

IR and OR may also be used as status signals indicating that the FIFO is completely full (IR stays LOW for at least t_{BT}) or completely empty (OR stays LOW for at least t_{BT}).

Reset

When master reset ($\overline{MR}$) goes LOW, the control logic is cleared, and the data outputs enter a LOW state. When $\overline{MR}$ returns HIGH, OR stays LOW, and IR goes HIGH if SI was LOW.

Logic Block Diagram



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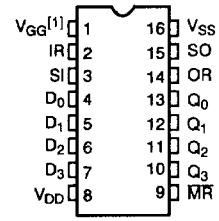
Pin Configuration



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Note:
1. Internally not connected.

Selection Guide

		3341	3341-2
Maximum Operating Frequency		1.2 MHz	2.0 MHz
Maximum Operating Current (mA)	Commercial	45	45
	Military	60	60

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage to Ground Potential (Pin 16 to Pin 8) ..... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to +7.0V

DC Input Voltage ..... − 3.0V to +7.0V

Output Current, into Outputs (Low) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}[1]
Commercial	0°C to +70°C	5V ±10%	GND	NC
Military[2]	− 55°C to +125°C	5V ±10%	GND	NC

Electrical Characteristics Over the Operating Range[3]

Parameters	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{SS} = Min., I_{OH} = − 0.3 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{SS} = Min., I_{OL} = 1.6 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{SS}	V
V_{IL}	Input LOW Voltage			− 3.0	0.8	V
I_{IX}	Input Leakage Current	$V_{DD} \le V_I \le V_{SS}$		− 10	+10	µA
I_{OS}	Output Short Circuit Current[4]	V_{SS} = Max., V_{OUT} = V_{DD}			− 90	mA
I_{DD}	Power Supply Current	V_{SS} = Max., I_{OUT} = 0 mA	Commercial		45	mA
			Military		60	
I_{GG}	V_{GG} Current				0	mA

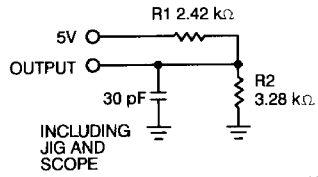
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{SS} = 5.0V	7	pF
C_{OUT}	Output Capacitance		10	pF

Notes:

2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



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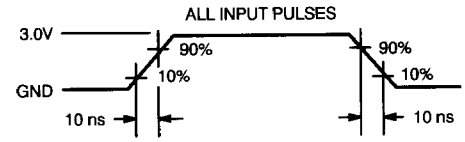

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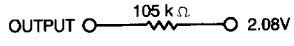
Equivalent to: THEVENIN EQUIVALENT



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Switching Characteristics Over the Operating Range[3, 6]

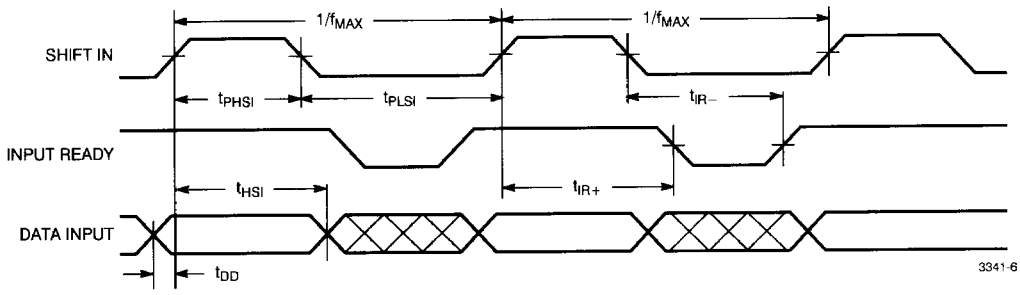
Parameters	Description	Test Conditions	3341		3341–2		Units
			Min.	Max.	Min.	Max.	
f_{MAX}	Operating Frequency	Note 7		1.2		2	MHz
t_{PHSI}	SI HIGH Time		80		80		ns
t_{PLSI}	SI LOW Time		80		80		ns
t_{DD}	Data Set-Up to SI		0		0		ns
t_{HSI}	Data Hold from SI		200		100		ns
t_{IR+}	Delay, SI HIGH to IR LOW		20	350	20	160	ns
t_{IR-}	Delay, SI LOW to IR HIGH		20	450	20	200	ns
t_{PHSO}	SO HIGH Time		80		80		ns
t_{PLSO}	SO LOW Time		80		80		ns
t_{OR+}	Delay, SO HIGH to OR LOW		20	370	20	160	ns
t_{OR-}	Delay, SO LOW to OR HIGH		20	450	20	200	ns
t_{DA}	Data Set-Up to OR HIGH		0		0		ns
t_{DH}	Data Hold from OR LOW		75		20		ns
t_{BT}	Bubble Through Time			1000		500	ns
t_{MRW}	$\overline{MR}$ Pulse Width		400		200		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		30		30		ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW			400		200	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH			400		200	ns

Notes:

6. Test conditions assume signal transition time of 10 ns or less, timing reference levels of 1.5V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
7. $1/f_{MAX} > t_{PHSI} + t_{IR-}$, $1/f_{MAX} > t_{PHSO} + t_{OR-}$.

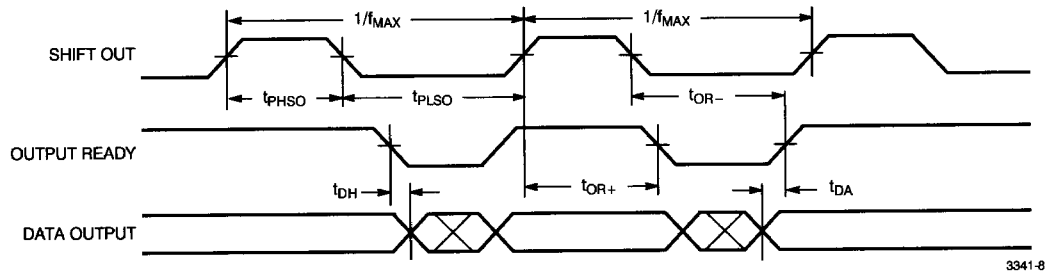
Switching Waveforms

Data In Timing Diagram

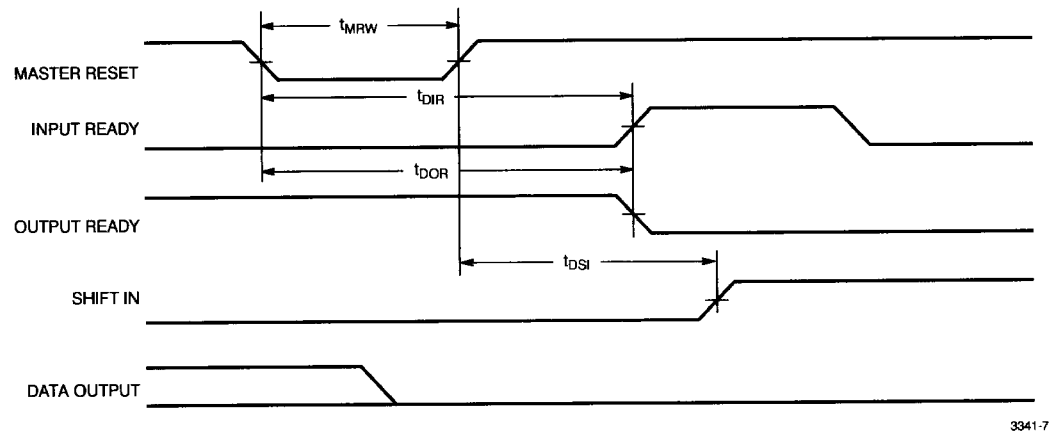


Switching Waveforms (Continued)

Data Out Timing Diagram



Master Reset Timing Diagram



Ordering Information

Ordering Code (1.2 MHz)	Package Type	Operating Range
CY3341PC	P1	Commercial
CY3341DC	D2	
CY3341DMB	D2	Military

Ordering Code (2 MHz)	Package Type	Operating Range
CY3341−2PC	P1	Commercial
CY3341−2DC	D2	
CY3341−2DMB	D2	Military

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{DD}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
f_{MAX}	7, 8, 9, 10, 11
t_{PHSI}	7, 8, 9, 10, 11
t_{PLSI}	7, 8, 9, 10, 11
t_{DD}	7, 8, 9, 10, 11
t_{HSI}	7, 8, 9, 10, 11
t_{IR+}	7, 8, 9, 10, 11
t_{IR-}	7, 8, 9, 10, 11
t_{PHSO}	7, 8, 9, 10, 11
t_{PLSO}	7, 8, 9, 10, 11
t_{OR+}	7, 8, 9, 10, 11
t_{OR-}	7, 8, 9, 10, 11
t_{DA}	7, 8, 9, 10, 11
t_{DH}	7, 8, 9, 10, 11
t_{BT}	7, 8, 9, 10, 11
t_{MRW}	7, 8, 9, 10, 11
t_{DSI}	7, 8, 9, 10, 11
t_{DOR}	7, 8, 9, 10, 11
t_{DIR}	7, 8, 9, 10, 11

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