

CD4070B, CD4077B

CMOS Quad Exclusive-OR and Exclusive-NOR Gate

Features

- High-Voltage Types (20V Rating)
- CD4070B - Quad Exclusive-OR Gate
- CD4077B - Quad Exclusive-NOR Gate
- Medium Speed Operation
 - t_{PHL} , t_{PLH} = 65ns (Typ) at V_{DD} = 10V, C_L = 50pF
- 100% Tested for Quiescent Current at 20V
- Standardized Symmetrical Output Characteristics
- 5V, 10V and 15V Parametric Ratings
- Maximum Input Current of 1 μ A at 18V Over Full Package Temperature Range
 - 100nA at 18V and 25°C
- Noise Margin (Over Full Package Temperature Range)
 - 1V at V_{DD} = 5V, 2V at V_{DD} = 10V, 2.5V at V_{DD} = 15V
- Meets All Requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications

- Logical Comparators
- Adders/Subtractors
- Parity Generators and Checkers

Description

The Harris CD4070B contains four independent Exclusive-OR gates. The Harris CD4077B contains four independent Exclusive-NOR gates.

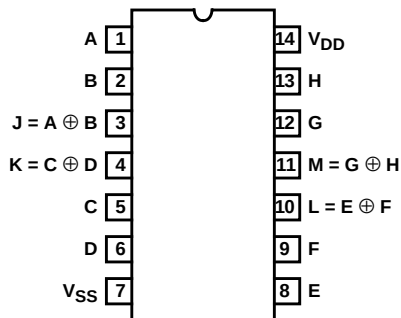
The CD4070B and CD4077B provide the system designer with a means for direct implementation of the Exclusive-OR and Exclusive-NOR functions, respectively.

Ordering Information

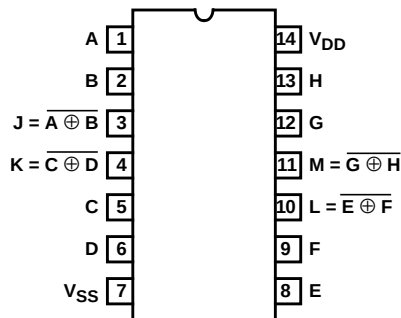
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD4070BE	-55 to 125	14 Ld PDIP	E14.3
CD4077BE	-55 to 125	14 Ld PDIP	E14.3
CD4070BF	-55 to 125	14 Ld Cerdip	F14.3
CD4077BF	-55 to 125	14 Ld Cerdip	F14.3
CD4070BM	-55 to 125	14 Ld SOIC	M14.15
CD4077BM	-55 to 125	14 Ld SOIC	M14.15

Pinouts

CD4070B
(PDIP, Cerdip, SOIC)
TOP VIEW



CD4077B
(PDIP, Cerdip, SOIC)
TOP VIEW



Functional Diagrams

CD4070B

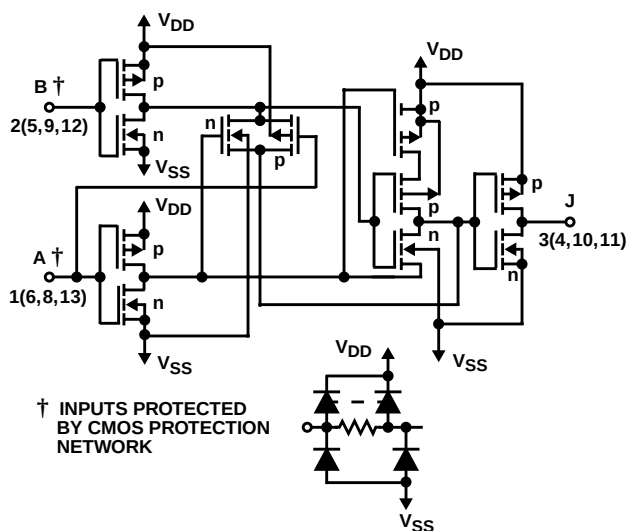
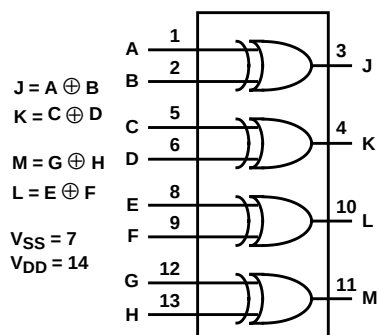


FIGURE 1. SCHEMATIC DIAGRAM FOR CD4070B
(1 OF 4 IDENTICAL GATES)

CD4070B TRUTH TABLE (1 OF 4 GATES)

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

NOTE:
 1 = High Level
 0 = Low Level
 $J = A \oplus B$

CD4077B

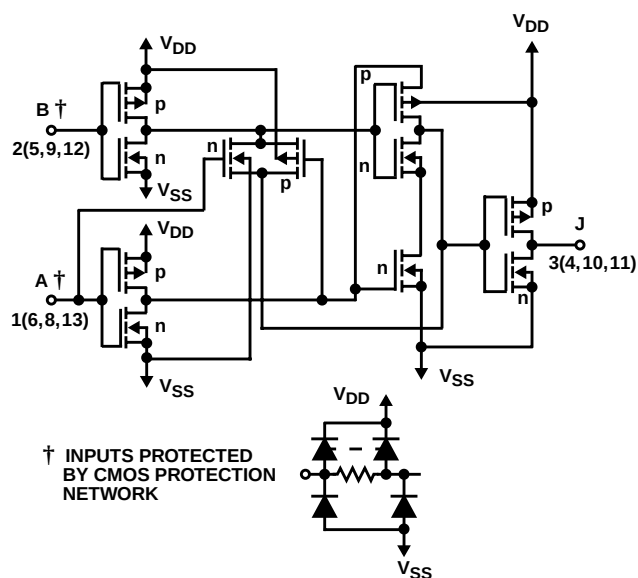
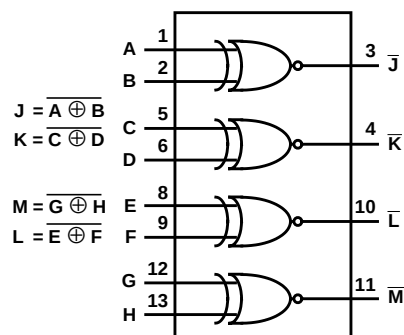


FIGURE 2. SCHEMATIC DIAGRAM FOR CD4077B
(1 OF 4 IDENTICAL GATES)

CD4077B TRUTH TABLE (1 OF 4 GATES)

A	B	J
0	0	1
1	0	0
0	1	0
1	1	1

NOTE:
 1 = High Level
 0 = Low Level
 $J = \overline{A \oplus B}$

CD4070B, CD4077B

Absolute Maximum Ratings

DC Supply Voltage Range (V_{DD}) -0.5V to 20V
 Input Voltage Range, All Inputs -0.5V to V_{DD} 0.5V
 DC Input Current $\pm 10\text{mA}$

Operating Conditions

Temperature Range (T_A) -55°C to 125°C
 Supply Voltage Range (Typical) 3V to 18V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W) θ_{JC} (°C/W)
 PDIP Package 90 N/A
 CERDIP Package 95 38
 SOIC Package 175 N/A
 Maximum Junction Temperature (Hermetic Package or Die) 175°C
 Maximum Junction Temperature (Plastic Package) 150°C
 Maximum Storage Temperature Range -65°C to 150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
					-55	-40	85	125	25		
	V _O (V)	V _{IN} (V)	V _{DD} (V)						MIN	TYP	
Quiescent Device Current I _{DD} Max	-	0, 5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	μA
	-	0, 10	10	0.5	0.5	15	15	-	0.01	0.5	μA
	-	0, 15	15	1	1	30	30	-	0.01	1	μA
	-	0, 20	20	5	5	150	150	-	0.02	5	μA
Output Low (Sink) Current I _{OL} Min	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	mA
	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	-	mA
Output High (Source) Current I _{OH} Min	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	mA
	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	mA
	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	mA
Output Voltage: Low Level, V _{OL} Max	-	0, 5	5	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0, 10	10	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0, 15	15	0.05	0.05	0.05	0.05	-	0	0.05	V
Output Voltage: High Level, V _{OH} Min	-	0, 5	5	4.95	4.95	4.95	4.95	4.95	5	-	V
	-	0, 10	10	9.95	9.95	9.95	9.95	9.95	10	-	V
	-	0, 15	15	14.95	14.95	14.95	14.95	14.95	15	-	V
Input Low Voltage, V _{IL} Max	0.5, 4.5	-	5	1.5	1.5	1.5	1.5	-	-	1.5	V
	1, 9	-	10	3	3	3	3	-	-	3	V
	1.5, 13.5	-	15	4	4	4	4	-	-	4	V
Input High Voltage, V _{IH} Min	0.5, 4.5	-	5	3.5	3.5	3.5	3.5	3.5	-	-	V
	1, 9	-	10	7	7	7	7	7	-	-	V
	1.5, 13.5	-	15	11	11	11	11	11	-	-	V
Input Current, I _{IN} Max	-	0, 18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

CD4070B, CD4077B

AC Electrical Specifications

$T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ns}$, $C_L = 50\text{pF}$, $R_L = 200\text{k}\Omega$

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS ON ALL TYPES		UNITS
		V_{DD} (V)	TYP	MAX	
Propagation Delay Time	t_{PHL}, t_{PLH}	5	140	280	ns
		10	65	130	ns
		15	50	100	ns
Transition Time	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	ns
		15	40	80	ns
Input Capacitance	C_{IN}	Any Input	5	7.5	pF

Typical Performance Curves

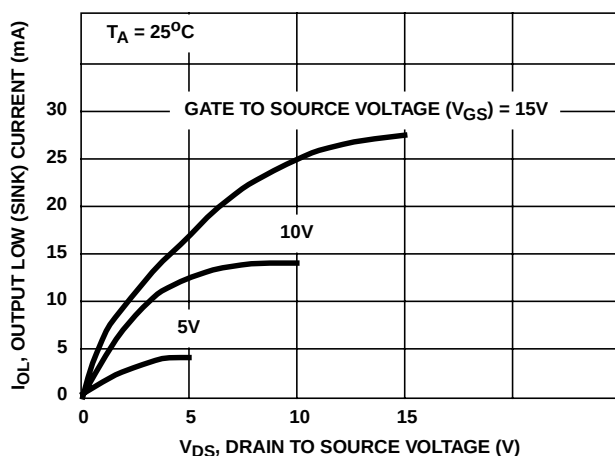


FIGURE 3. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

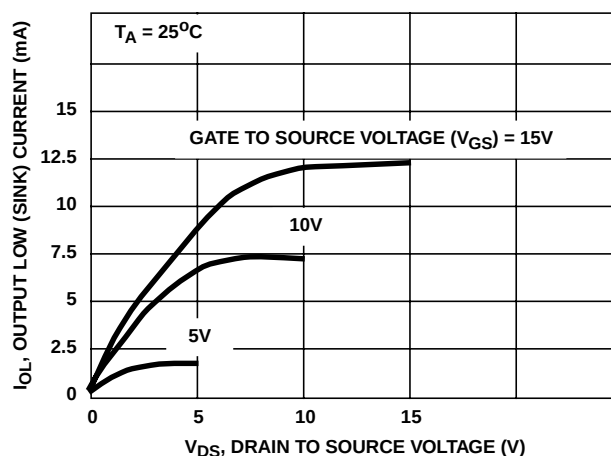


FIGURE 4. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

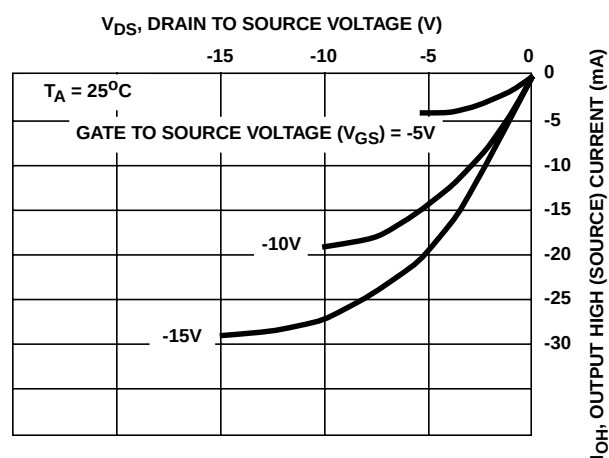


FIGURE 5. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

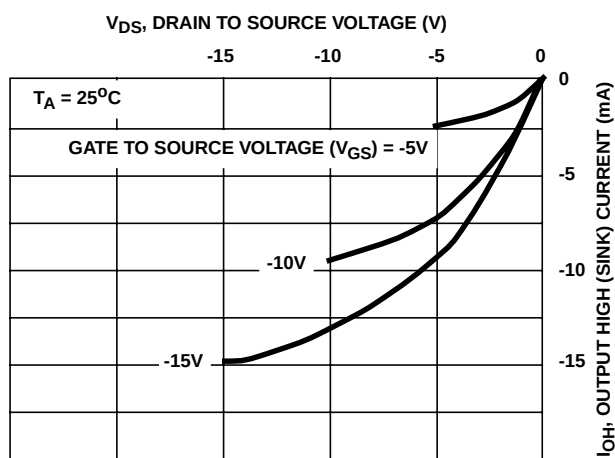


FIGURE 6. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

Typical Performance Curves (Continued)

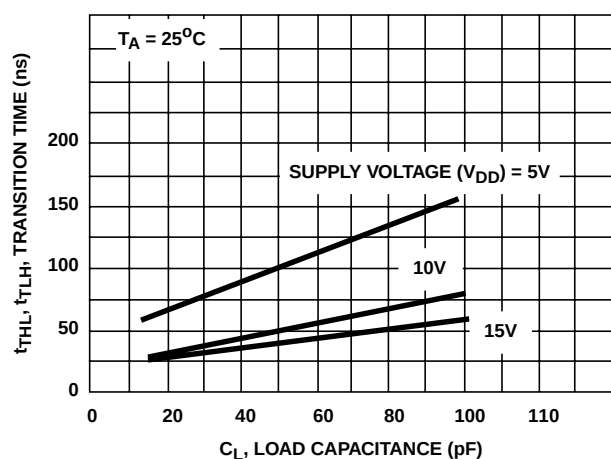


FIGURE 7. TYPICAL TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

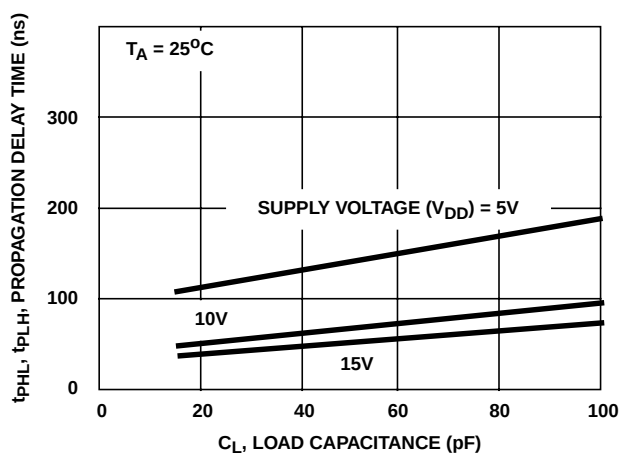


FIGURE 8. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE

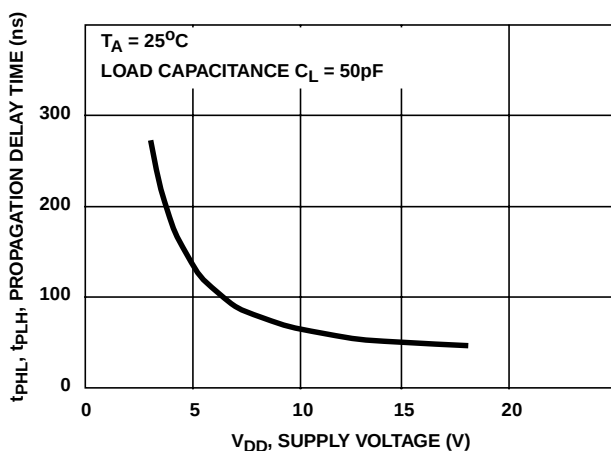


FIGURE 9. TYPICAL PROPAGATION DELAY TIME AS A FUNCTION OF SUPPLY VOLTAGE

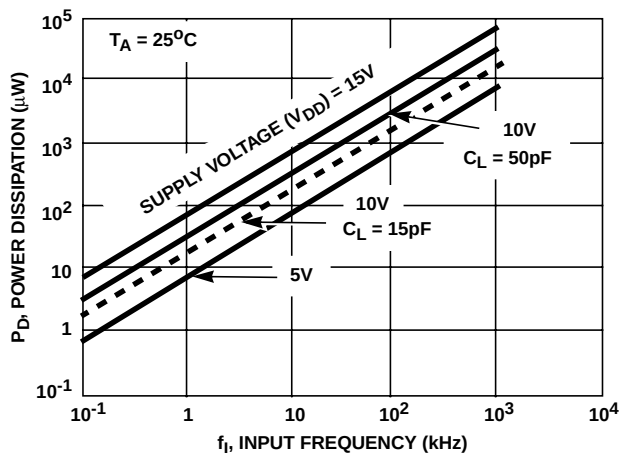
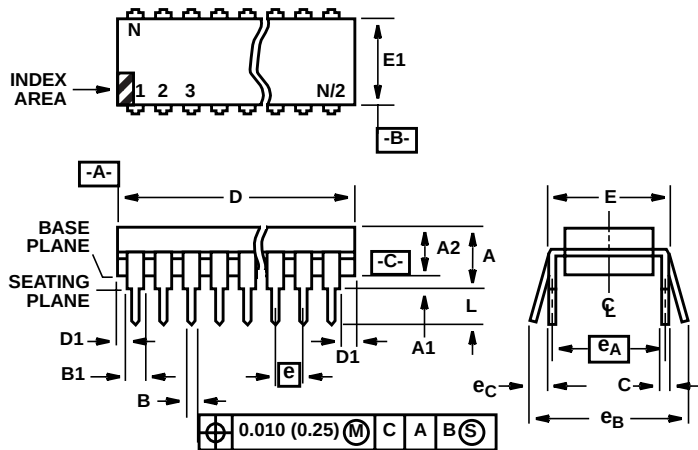


FIGURE 10. TYPICAL DYNAMIC POWER DISSIPATION AS A FUNCTION OF INPUT FREQUENCY

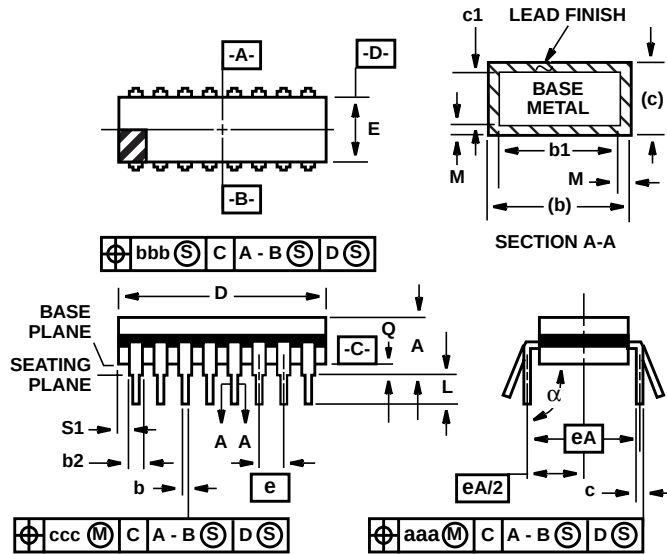
Dual-In-Line Plastic Packages (PDIP)**NOTES:**

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum C .
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)**14 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

**F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

Rev. 0 4/94

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.