

CMOS Dual 4-Stage Static Shift Register

With Serial Input/Parallel Output

High-Voltage Types (20-Volt Rating)

■ CD4015B consists of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015B package, or to more than 8 stages using additional CD4015B's is possible.

The CD4015B-series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

Features:

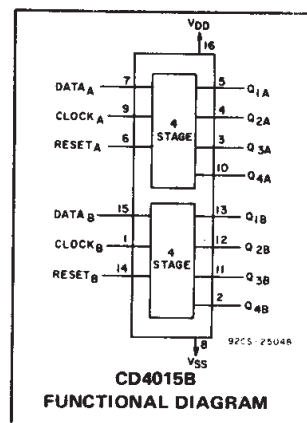
- Medium speed operation 12 MHz (typ.) clock rate at $V_{DD} - V_{SS} = 10\text{ V}$
- Fully static operation
- 8 master-slave flip-flops plus input and output buffering
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of $1\text{ }\mu\text{A}$ at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
 - 1 V at $V_{DD} = 5\text{ V}$
 - 2 V at $V_{DD} = 10\text{ V}$
 - 2.5 V at $V_{DD} = 15\text{ V}$

- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial-input/parallel-output data queueing
- Serial to parallel data conversion
- General-purpose register

CD4015B Types



TERMINAL DIAGRAM

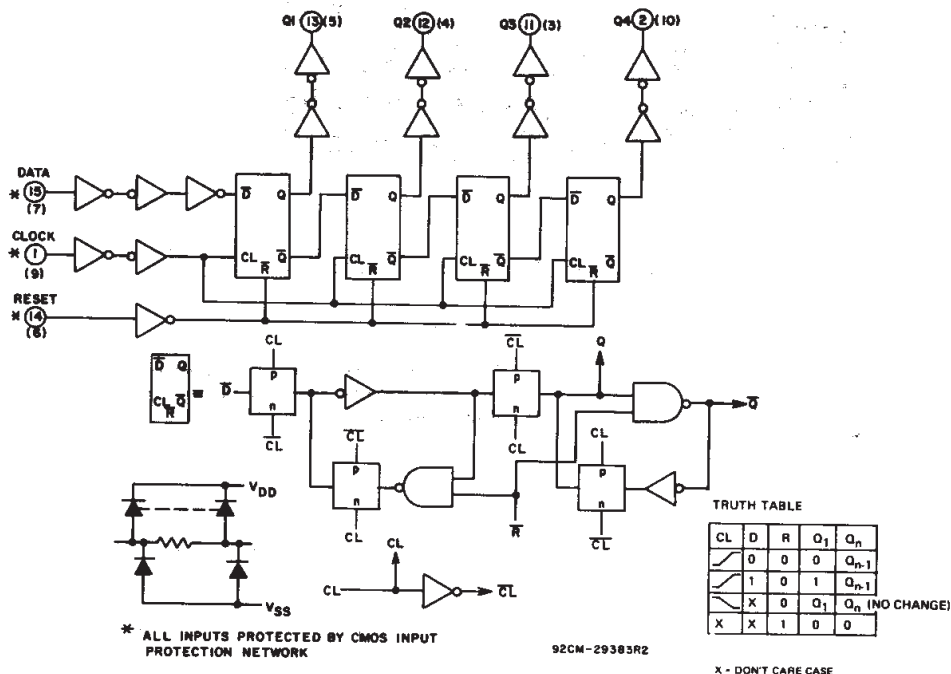
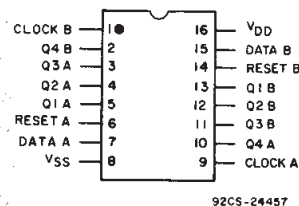


Fig. 1 — Logic diagram (1 register).

CD4015B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal)

-0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

-0.5V to $V_{DD} + 0.5V$

DC INPUT CURRENT, ANY ONE INPUT

$\pm 10mA$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ C$ to $+100^\circ C$

500mW

For $T_A = +100^\circ C$ to $+125^\circ C$

Derate Linearly at 12mW/ $^\circ C$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)

100mW

OPERATING-TEMPERATURE RANGE (T_A)

$-55^\circ C$ to $+125^\circ C$

STORAGE TEMPERATURE RANGE (T_{stg})

$-65^\circ C$ to $+150^\circ C$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max $+265^\circ C$

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ C$, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)		3	18	V
Clock Pulse Width, t_{WCL}	5	180	—	ns
	10	80	—	
	15	50	—	
Clock Rise and Fall Time, t_{rCL}, t_{fCL}	5	—	15	μs
	10	—	6	
	15	—	2	
Clock Input Frequency, f_{CL}	5	—	3	MHz
	10	DC	6	
	15	—	8.5	
Data Setup Time, t_{SU}	5	70	—	ns
	10	40	—	
	15	30	—	
Reset Pulse Width, t_{WR}	5	200	—	ns
	10	80	—	
	15	60	—	

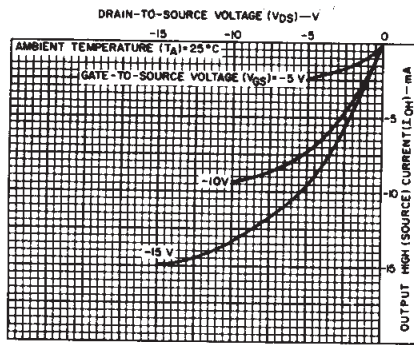


Fig. 5 — Minimum output high (source) current characteristics.

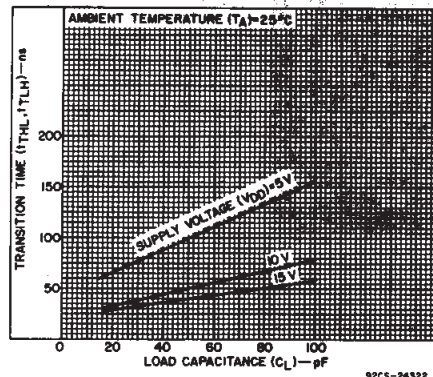


Fig. 6 — Typical transition time as a function of load capacitance.

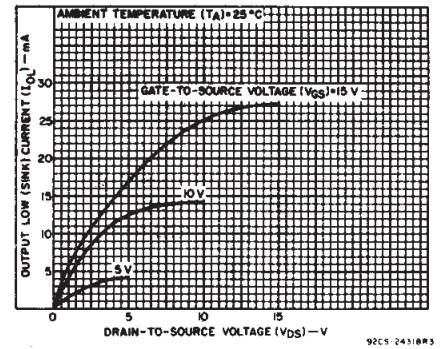


Fig. 2 — Typical output low (sink) current characteristics.

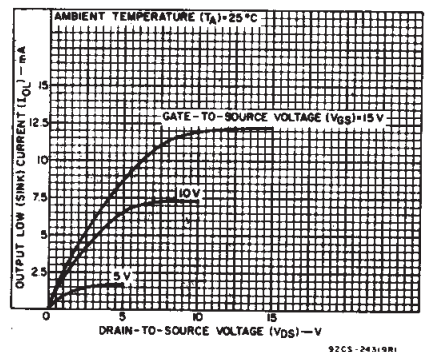


Fig. 3 — Minimum output low (sink) current characteristics.

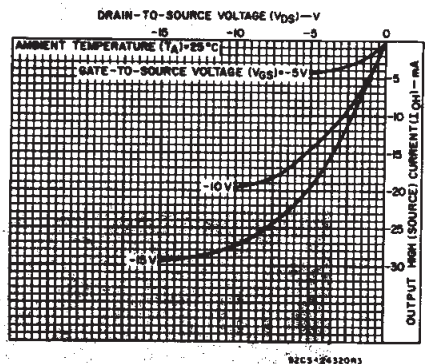


Fig. 4 — Typical output high (source) current characteristics.

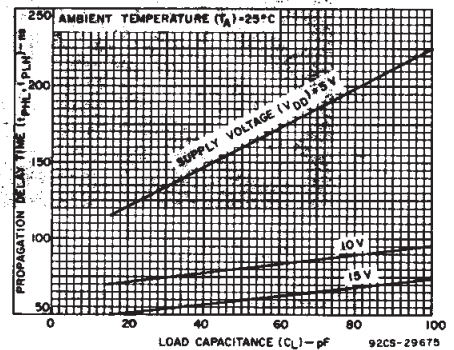


Fig. 7 — Typical propagation delay time as a function of load capacitance.

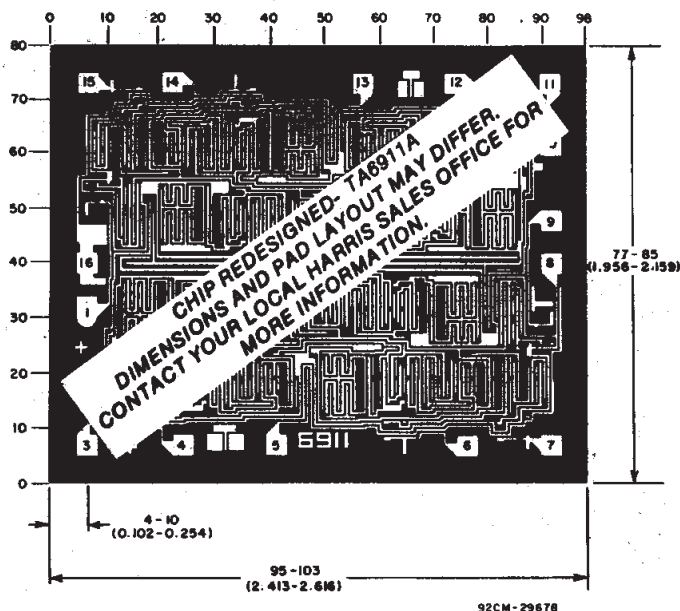
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COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4015B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)					+25			
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V _{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	—	0,5	5	4.95				4.95	5	—	V
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	—	5	3.5				3.5	—	—	V
	1, 9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I _{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 ⁻⁵	±0.1	μA



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

Photograph of Chip Layout for CD4015B.

CD4015B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS V _{OD} (V)	LIMITS			UNITS
		MIN.	TYP.	MAX.	
CLOCKED OPERATION					
Propagation Delay Time, T _{PHL} , T _{PLH}	5	—	160	320	ns
	10	—	80	160	
	15	—	60	120	
Transition Time, t _{THL} , t _{TLH}	5	—	100	200	
	10	—	50	100	
	15	—	40	80	
Minimum Clock Pulse Width, t _{wCL}	5	—	90	180	
	10	—	40	80	
	15	—	25	50	
Clock Rise and Fall Time, t _{rCL} , t _{fCL} *	5	—	—	15	μs
	10	—	—	6	
	15	—	—	2	
Minimum Data Setup Time, t _{SU}	5	—	35	70	ns
	10	—	20	40	
	15	—	15	30	
Minimum Data Hold Time, t _H	5	—	—	0	
	10	—	—	0	
	15	—	—	0	
Maximum Clock Input Frequency, f _{CL}	5	3	6	—	MHz
	10	6	12	—	
	15	8.5	17	—	
Input Capacitance, C _{IN}	Any Input	—	5	7.5	pF
RESET OPERATION					
Propagation Delay Time, T _{PHL} , T _{PLH}	5	—	200	400	ns
	10	—	100	200	
	15	—	80	160	
Minimum Reset Pulse Width, t _{wR}	5	—	100	200	
	10	—	40	80	
	15	—	30	60	

*If more than one unit is cascaded t_{rCL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

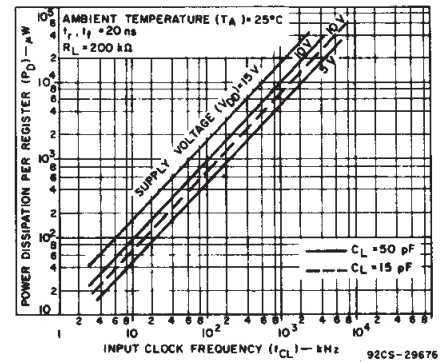


Fig. 8 — Typical power dissipation as a function of frequency.

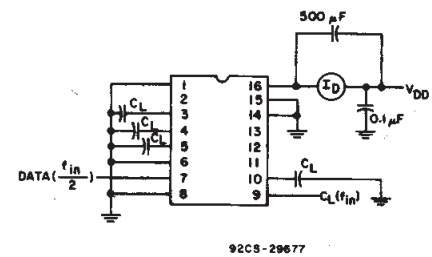


Fig. 9 — Power dissipation test circuit.

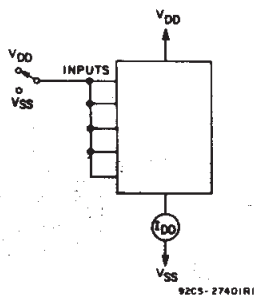


Fig. 10 — Quiescent device current test circuit.

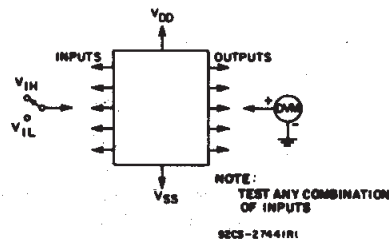


Fig. 11 — Input voltage test circuit.

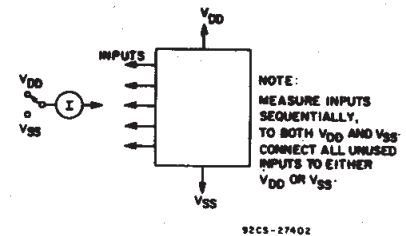


Fig. 12 — Input current test circuit.

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