Bolymin, Inc.

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LCD MODULE SPECIFICATION

MODEL NO.

BC1602E series

FOR MESSRS:

_____

ON DATE OF:

_____

APPROVED BY:

_____

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C O N T E N T S

Bolymin, Inc.

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1. Numbering System

	B	C	1602	E	-	-	-	-	-	xxx
	0	1	2	3	4	5	6	7	8	9

0	Brand		Bolymin	
1	Module Type		C= character type G= graphic type P= TAB/TCP type	O= COG type F= COF type
2	Format		2002=20 characters, 4 lines 12232= 122 x 32 dots	
3	Version No.		A type	
4	LCD Color		G=STN/gray Y=STN/yellow-green C=color STN	B=STN/blue F=FSTN T=TN
5	LCD Type		R=positive/reflective P=positive/transflective	M=positive/transmissive N=negative/transmissive
6	Backlight type/color		L=LED array/ yellow-green H=LED edge/white R=LED array/red G=LED edge/yellow-green	D=LED edge/blue E=EL/white B=EL/blue C=CCFL/white
7	CGRAM Font		J=English/Japanese Font E=English/European Font	C=English/Cyrillic Font H=English/Hebrew Font
8	View Angle/ Operating Temperature		B=Bottom/Normal Temperature H=Bottom/Wide Temperature U=Bottom/Ultra wide Temperature	T=Top/Normal Temperature W=Top/Wide Temperature C=9H/Normal Temperature
9	Special Code		3=3 volt logic power supply n=negative voltage for LCD c=cable/connector xxx=to be assigned on data sheet	t=temperature compensation for LCD p=touch panel $=RoHS

2. Precaution in use of LCD Module

(1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.

(2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.

(3) Don't disassemble the LCM.

(4) Don't operate it above the absolute maximum rating.

(5) Don't drop, bend or twist LCM.

(6) Soldering: only to the I/O terminals.

(7) Storage: please storage in anti-static electricity container and clean environment.

(8)Don't touch the elastmer connecter, especially insert a backlight panel(EL or CCFL)

3. General Specification

(1) Mechanical Dimension

Item	Dimension	Unit
Number of Characters	16characters x 2 Lines	—
Module dimension (L x W x H)	122.2 x 44.0 x 13.1 (Max)– LED B/L LED edge B/L(white, blue) 122.2 x 44.0 x 9.3 (Max/) – EL or No B/L	mm
View area	99.0 x 24.0	mm
Active area	94.84 x 20.0	mm
Dot size	0.92 x 1.1	mm
Dot pitch	0.98 x 1.16	mm
Character size (L x W)	4.84 x 8.06	mm
Character pitch (L x W)	6.0 x 9.66	mm

(2) Controller IC: **KS0066 (or Equivalent) controller**

(3) Temperature Range

	Normal	Wide
Operating	0 ~+50℃	-20 ~+70℃
Storage	-10 ~+ 60℃	-30 ~+80℃

4. Absolute Maximum Ratings

4.1 Electrical Absolute Maximum Ratings

(Vss=0V, Ta=25℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage For Logic	Vdd-Vss	-0.3	—	7	V
Supply Voltage For LCD	Vdd-Vo	-0.3	—	5.5	V
Input Voltage	VI	Vss	—	Vdd	V
Normal Type	TOP	0	—	+50	℃
	Tstg	-10	—	+60	℃
Wide Temperature Type	Top	-20	—	+70	℃
	Tstg	-30	—	+80	℃

5. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	Vdd-Vss	—	3.0	—	5.5	V
Supply Voltage For LCD ＊Wide Temp、Type	Vdd-Vo	＊Ta=-20℃	—	5.0	—	V
		Ta=0℃	—	—	—	V
		Ta=25℃	—	**4.2**	—	V
		Ta=50℃	—	—	—	V
		＊Ta=+70℃	—	3.8	—	V
Input High Volt.	V_{IH}	—	2.2	—	Vdd	V
Input Low Volt.	V_{IL}	—	—	—	0.6	V
Output High Volt.	V_{OH}	—	2.4	—	—	V
Output Low Volt.	V_{OL}	—	—	—	0.4	V
Supply Current	Idd	Vdd=5V	—	1.2	—	mA

6. Optical Characteristics

a. STN

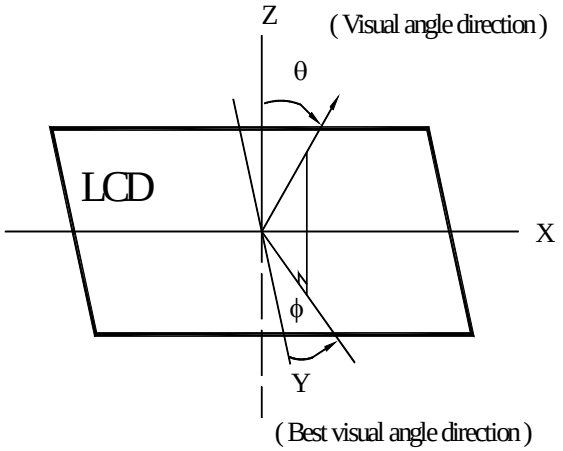
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
View Angle	(V) θ	CR≧2	10		45	deg
	(H) φ	CR≧2	-30		30	deg
Contrast Ratio	CR	—		3		—
Response Time 25℃	T rise	—		100	150	ms
	T fall	—		150	200	ms

b. FSTN

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
View Angle	(V) θ	CR≧3	10		60	deg
	(H) φ	CR≧3	-45		45	deg
Contrast Ratio	CR	—		5		—
Response Time 25℃	T rise	—		100	150	ms
	T fall	—		150	200	ms

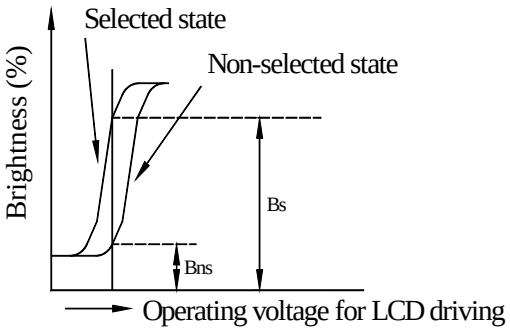
6.1 Definitions

■View Angles

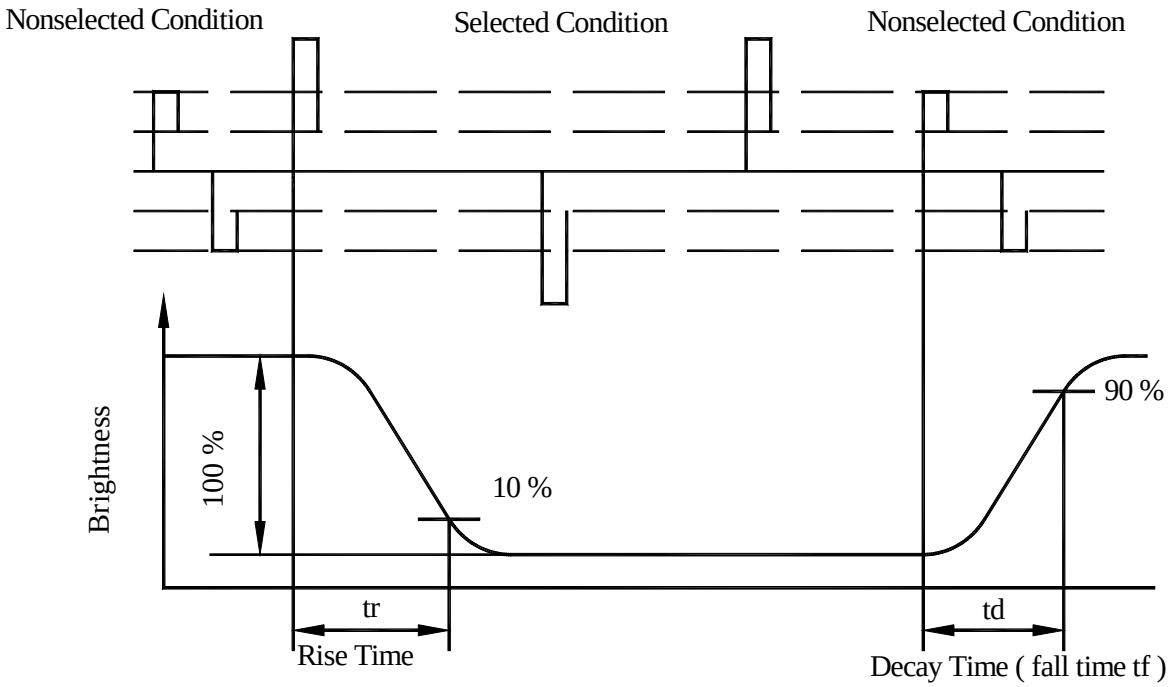


■Contrast Ratio

$$CR = \frac{\text{Brightness at selected state (BS)}}{\text{Brightness at non-selected state (Bns)}}$$



■Response Time

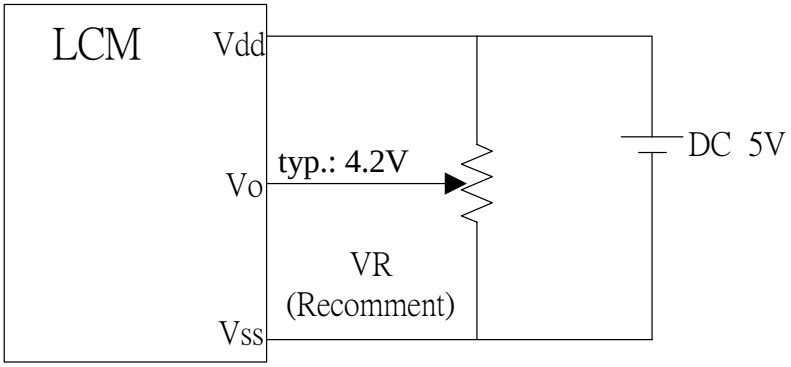


7. Interface Pin Function

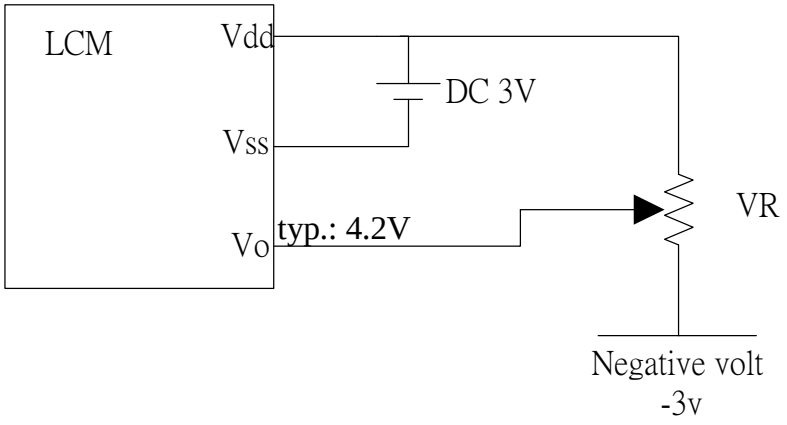
Pin No.	Symbol	Level	Description
1	Vss	0V	Ground
2	Vdd	5.0V	Supply Voltage for logic **(option +3.0V)**
3	Vo	(Variable)	Operating voltage for LCD
4	RS	H/L	H: DATA, L: Instruction code
5	R/W	H/L	H: Read(MPU→Module) L: Write(MPU→Module)
6	E	H,H→L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	A / Vee	—	Power supply for LED backlight (+) / Negative voltage output (optional)
16	K	—	Power supply for LED backlight (-)

8. Power Supply for LCD Module and LCD Operating Voltage a Adjustment

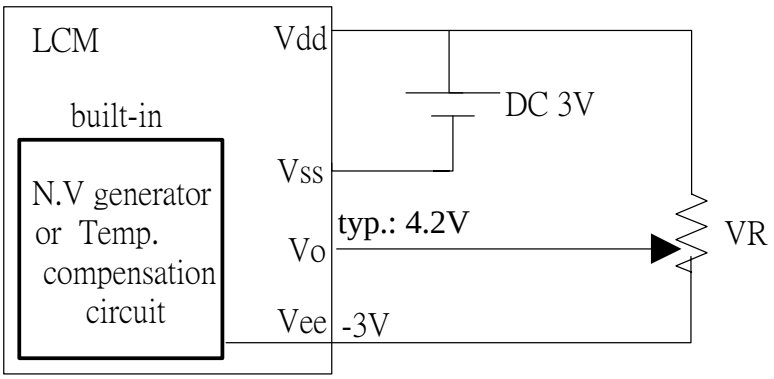
＊Standard Type



＊(Option)LCM operating on " DC 3V " input with external negative voltage



＊(Option) LCM operating on " DC 3V " input with built-in negative voltage



9.Backlight Information

9. 1 Specification

(1) LED array / yellow-green

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Current	ILED	—	280	—	mA	V=4.2V
Supply Voltage	V	—	4.2	4.3	V	—
Reverse Voltage	VR	—	—	8	V	—
Luminous Intensity	IV	60	—	—	cd/m^2	ILED=280mA
Wave Length	λp	—	574	—	nm	ILED=280mA
Life Time	—	—	100000	—	Hr.	ILED≦280mA
Color	Yellow Green					

(1) LED array /red

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Current	ILED	—	280	—	mA	V=3.9V
Supply Voltage	V	—	3.9	4.0	V	—
Reverse Voltage	VR	—	—	8	V	—
Luminous Intensity	IV	30	35	—	cd/m^2	ILED=280mA
Wave Length	λp	—	665	—	nm	ILED=280mA
Life Time	—	—	30000	—	Hr.	ILED≦280mA
Color	Red					

(2) LED edge/ white or blue

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Current	ILED	—	20	30	mA	V=3.2V
Supply Voltage	V	—	3.2	3.3	V	
Reverse Voltage	VR	—	—	8	V	
Luminous Intensity	IV	50	—	—	cd/m^2	ILED≦20mA
Life Time		—	35000	—	Hr.	ILED≦20mA
Color	White(Blue)					

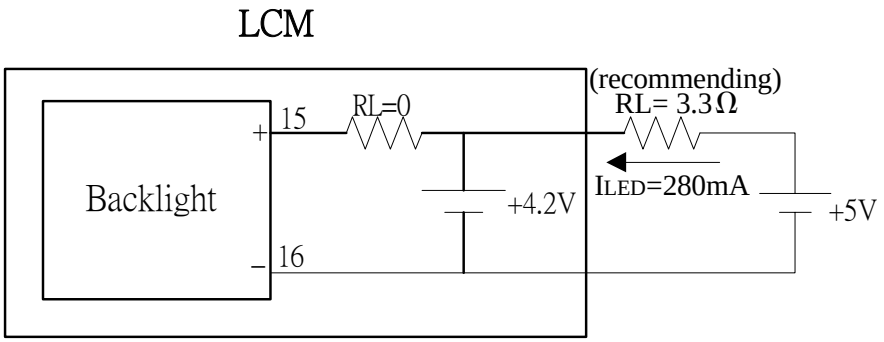
(3) EL /White(blue)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Voltage	Vrms	--	110 (AC)		--	
Frequency	HZ	--	400		--	
Brightness*	cd/m^2	48	60		--	110Vrms 400Hz
CIE Chromaticity Diagram	X	--	0.2901white 0.182 blue		--	
	Y	--	0.3608 white 0.46 blue		--	
Current Dissipation	mA/cm^2	--	1.33		--	
Power Dissipation	mW/cm^2	--	26.29		--	
Color	White(Blue)					

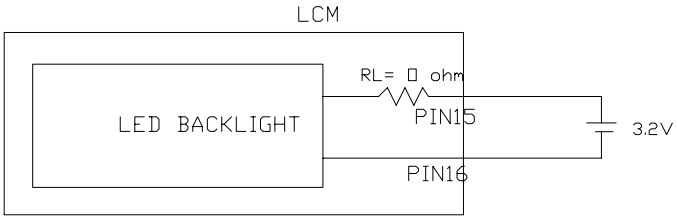
9.2 Backlight driving methods

a. LED B/L drive from pin15 (LED+) pin16 (LED-)

a.1 array / yellow-green

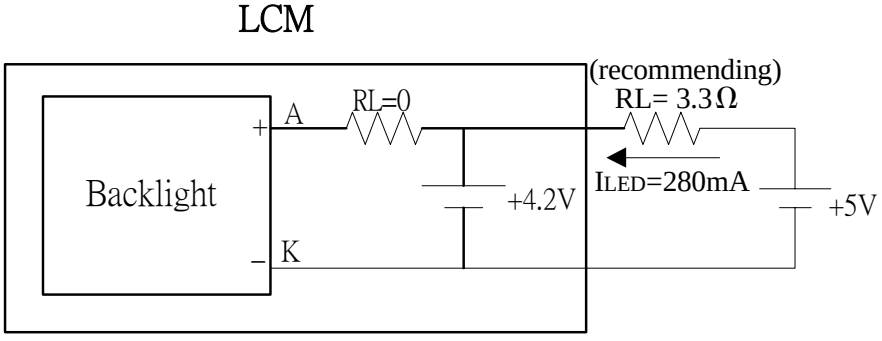


a.2 LED white or blue

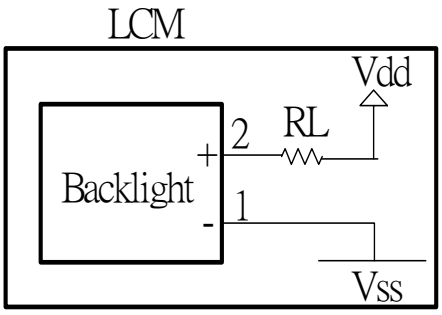


b. LED B/L drive from A.K directly

b.1 array / yellow-green

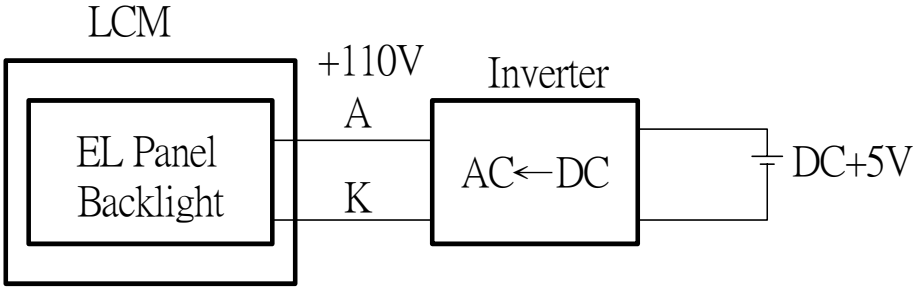


c. ∗ (Option) LED B/L drive from pin1 (Vss) pin2 (Vdd)



(1) Jump 1,2 Short
(2) Current Resistor required on RL
(3) Jump 15,16 open
(4) To be sure of enough current supply for both Vdd + LED B/L

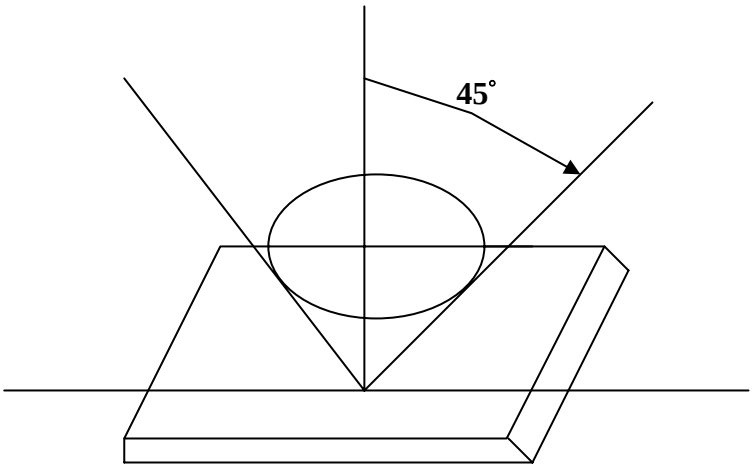
d. E/L B/L driven from A.K cable directly



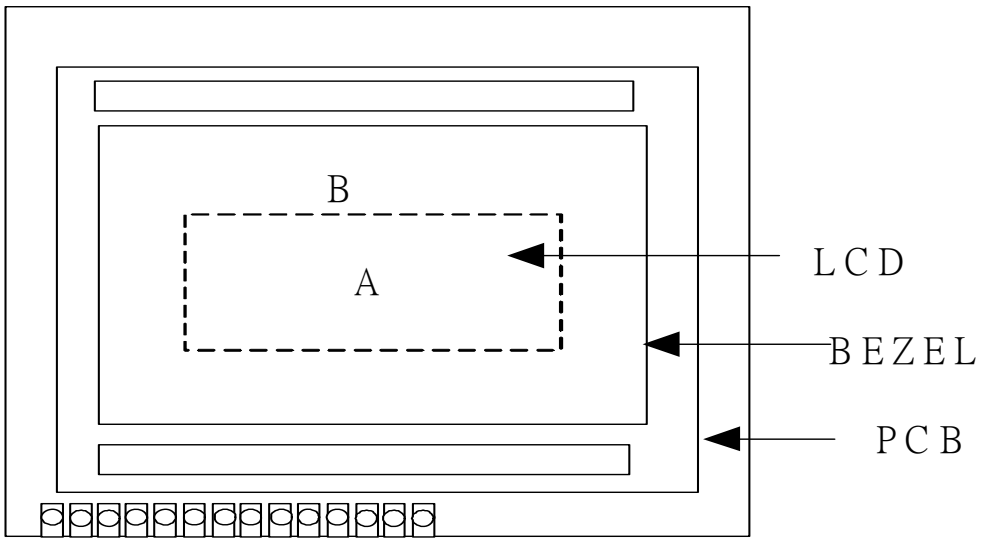
10. Quality Assurance

10.1 Inspection conditions

The LCD shall be inspected under 40W white fluorescent light.



Definition of applicable Zones

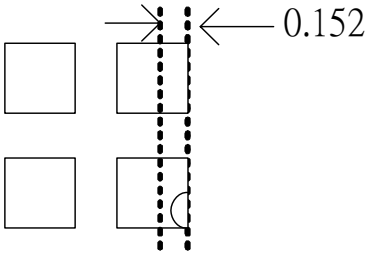
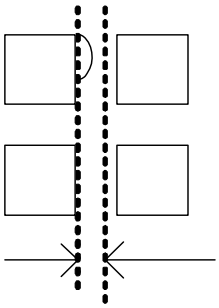
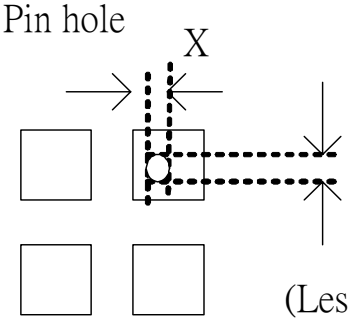
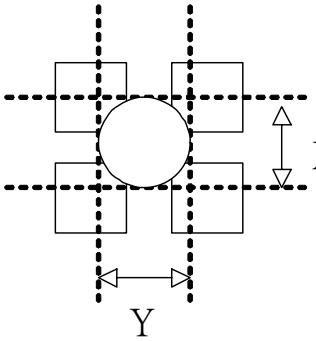


A : Display Area

B : Non-Display Area

10.2 Inspection Parameters

<table>
<tr><th>NO.</th><th>Parameter</th><th>Criteria</th></tr>
<tr><td>1</td><td>Black or White spots</td><td>
<table>
<tr><th>Zone / Dimension</th><th colspan="2">Acceptable Number</th><th>Class Of Defects</th><th>Acceptable Level</th></tr>
<tr><th></th><th>A</th><th>B</th><th></th><th></th></tr>
<tr><td>D＜0.15</td><td>*</td><td>*</td><td rowspan="4">Minor</td><td rowspan="4">2.5</td></tr>
<tr><td>0.15≦D≦0.2</td><td>4</td><td>4</td></tr>
<tr><td>0.2≦D≦0.25</td><td>2</td><td>2</td></tr>
<tr><td>D≦0.3</td><td>0</td><td>1</td></tr>
</table>
D=(Long + Short)/2 *: Disregard
</td></tr>
<tr><td>2</td><td>Scratch, Substances</td><td>
<table>
<tr><th colspan="2">Zone
X(mm) Y(mm)</th><th colspan="2">Acceptable Number</th><th>Class Of Defects</th><th>Acceptable Level</th></tr>
<tr><th></th><th></th><th>A</th><th>B</th><th></th><th></th></tr>
<tr><td>*</td><td>0.04≧W</td><td>*</td><td>*</td><td rowspan="4">Minor</td><td rowspan="4">2.5</td></tr>
<tr><td>3.0≧L</td><td>0.06≧W</td><td>4</td><td>4</td></tr>
<tr><td>2.0≧L</td><td>0.08≧W</td><td>2</td><td>3</td></tr>
<tr><td>－</td><td>0.1＜W</td><td>0</td><td>1</td></tr>
</table>
X: Length Y: Width *: Disregard
Total defects should not exceed 4/module
</td></tr>
<tr><td>3</td><td>Air Bubbles (between glass & polarizer)</td><td>
<table>
<tr><th>Zone / Dimension</th><th colspan="2">Acceptable Number</th><th>Class Of Defects</th><th>Acceptable Level</th></tr>
<tr><th></th><th>A</th><th>B</th><th></th><th></th></tr>
<tr><td>D≦0.15</td><td>*</td><td>*</td><td rowspan="3">Minor</td><td rowspan="3">2.5</td></tr>
<tr><td>0.15＜D≦0.25</td><td>2</td><td>*</td></tr>
<tr><td>0.25＜D</td><td>0</td><td>1</td></tr>
</table>
*: Disregard
Total defects shall not excess 3/module.
</td></tr>
</table>

4	Uniformity	(1) Pixel shape (with Dent)  (2) Pixel shape (With Projection)  Should not be connected to next pixel 0.152 (3) Pin hole  (X+Y)/2≦0.02mm (Less than 0.1mm is no counted) (4)Deformation  (X+Y)/2 ≦0.3mm Total acceptable number : 1/pixel,5/cell

11.Reliability

■Content of Reliability Test

Environmental Test				
No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High Temperature storage	Endurance test applying the high storage temperature for a long time.	60℃ 200hrs	——
2	Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-20℃ 200hrs	——
3	High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50℃ 200hrs	——
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	0℃ 200hrs	——
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60℃,90%RH 96hrs	——
6	High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40℃,90%RH 96hrs	——
7	Temperature Cycle	Endurance test applying the low and high temperature cycle. -20℃ 25℃ 60℃ 30min 5min 30min 1 cycle	-20℃/60℃ 10 cycles	——
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	——
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msedc 3 times of each direction	——
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	——
Others				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	——

***Supply voltage for logic system=5V. Supply voltage for LCD system =Operating voltage at 25℃

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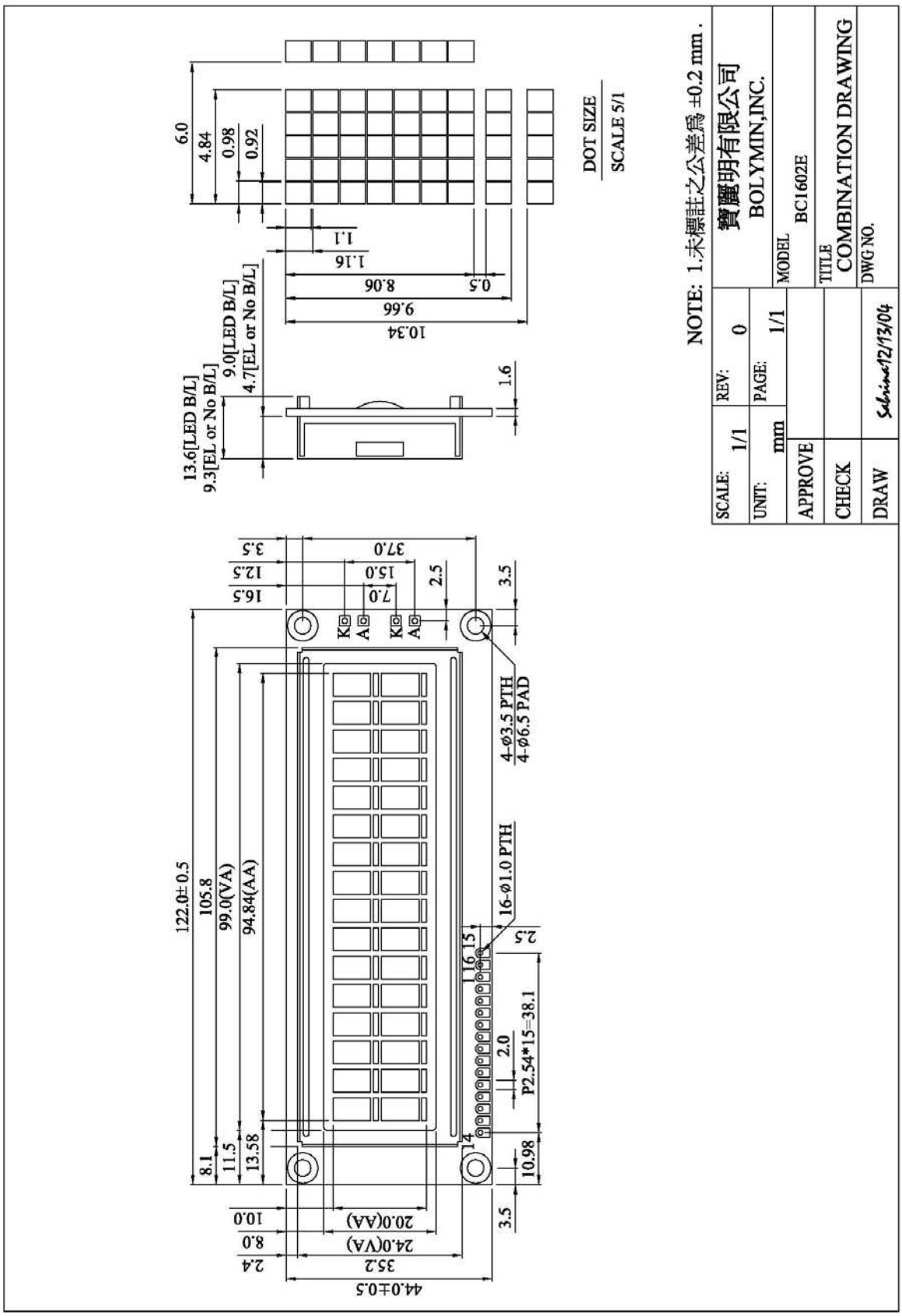
12. Appendix (Drawing , EL inverter data , KS0066 controller data)



12-2. KS0066 controller data

12-2.1 Function description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

Busy Flag (BF)

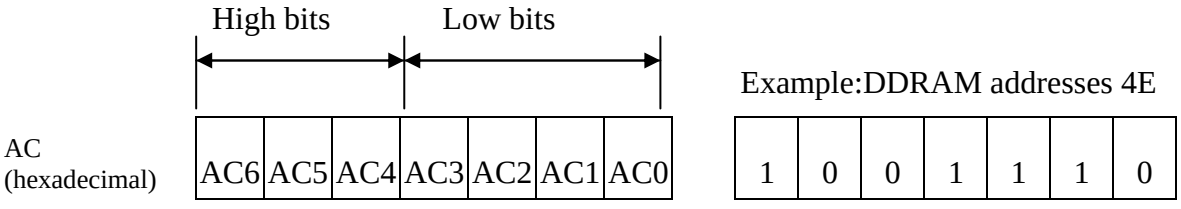
When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationship between DDRAM addresses and positions on the liquid crystal display.



DDRAM Address

Display position DDRAM address

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

Example: 2-Line by 16-Character Display

Character Generator ROM (CGROM)

The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See Table 2.

Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns can be written, and for 5×10 dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data)

For 5 * 8 dot character patterns

Character Codes (DDRAM data)	CGRAM Address	Character Patterns (CGRAM data)	
7 6 5 4 3 2 1 0 (High Low)	5 4 3 2 1 0 (High Low)	7 6 5 4 3 2 1 0 (High Low)	
0 0 0 0 * 0 0 0	0 0 0	0 0 0	Character pattern(1)
		0 0 1	
		0 1 0	
		0 1 1	
		1 0 0	
		1 0 1	
		1 1 0	
		1 1 1	Cursor pattern
0 0 0 0 * 0 0 1	0 0 1	0 0 0	Character pattern(2)
		0 0 1	
		0 1 0	
		0 1 1	
		1 0 0	
		1 0 1	
		1 1 0	
		1 1 1	Cursor pattern
		0 0 0	
		0 0 1	
0 0 0 0 * 1 1 1	1 1 1	1 0 0	
		1 0 1	
		1 1 0	
		1 1 1	

For 5 * 10 dot character patterns

Character Codes (DDRAM data)	CGRAM Address	Character Patterns (CGRAM data)	
7 6 5 4 3 2 1 0 (High Low)	5 4 3 2 1 0 (High Low)	7 6 5 4 3 2 1 0 (High Low)	
0 0 0 0 * 0 0 0	0 0 0 0 0	0 0 0 0 0	Character pattern
	0 0 0 1	0 0 0 0 0	
	0 0 1 0	0 0 0 0 0	
	0 0 1 1	0 0 0 0 0	
	0 1 0 0	0 0 0 0 0	
	0 1 0 1	0 0 0 0 0	
	0 1 1 0	0 0 0 0 0	
	0 1 1 1	0 0 0 0 0	
	1 0 0 0	0 0 0 0 0	
	1 0 0 1	0 0 0 0 0	
	1 0 1 0	0 0 0 0 0	Cursor pattern
	1 1 1 1	* * * * * * * *	

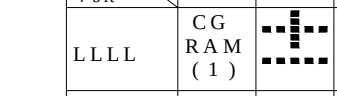
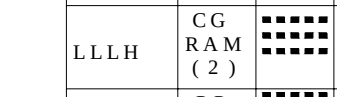
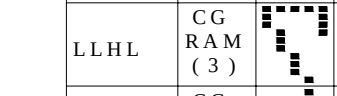
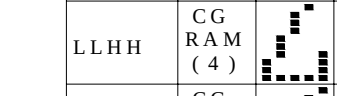
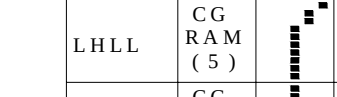
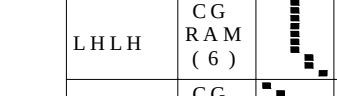
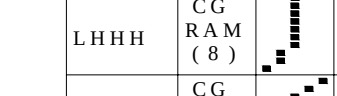
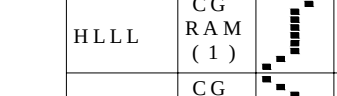
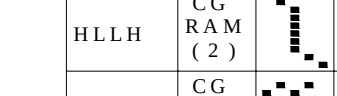
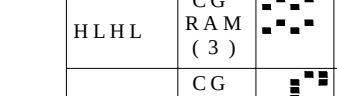
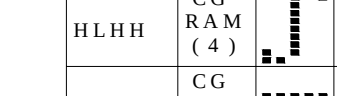
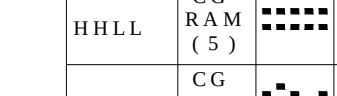
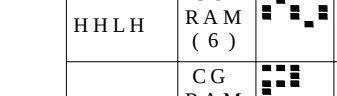
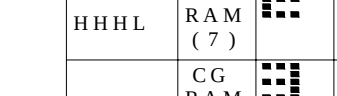
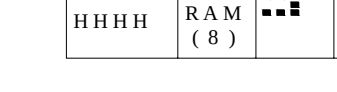
■ : " High "

12-2.2 C.G ROM table. table 2

Code J: English – Japanese Font

Upper 4 bit / Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

Code E: English - European Font

Upper 4 bit / Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	CG RAM (2)															
LLHL	CG RAM (3)															
LLHH	CG RAM (4)															
LHLL	CG RAM (5)															
LHLH	CG RAM (6)															
LHHL	CG RAM (7)															
LHHH	CG RAM (8)															
HLLL	CG RAM (1)															
HLLH	CG RAM (2)															
HLHL	CG RAM (3)															
HLHH	CG RAM (4)															
HHLL	CG RAM (5)															
HHLH	CG RAM (6)															
HHHL	CG RAM (7)															
HHHH	CG RAM (8)															

Code C: English - Cyrillic Font

Upper 4 bit / Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	CG RAM (2)															
LLHL	CG RAM (3)															
LLHH	CG RAM (4)															
LHLL	CG RAM (5)															
LHLH	CG RAM (6)															
LHHL	CG RAM (7)															
LHHH	CG RAM (8)															
HLLL	CG RAM (1)															
HLLH	CG RAM (2)															
HLHL	CG RAM (3)															
HLHH	CG RAM (4)															
HHLL	CG RAM (5)															
HHLH	CG RAM (6)															
HHHL	CG RAM (7)															
HHHH	CG RAM (8)															

◆◆◆

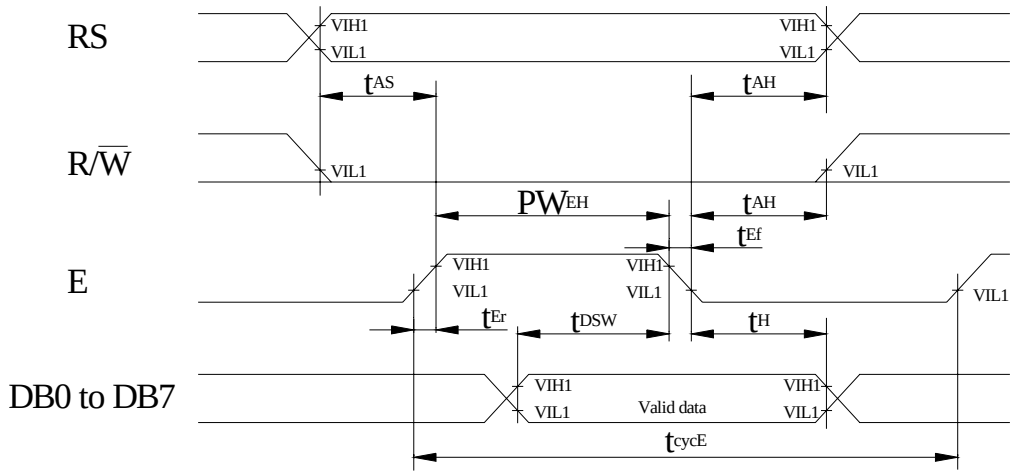
12-2.3 Instruction table

Instruction	Instruction Code										Description	Execution time (fosc=270Khz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “00H” to DDRAM and set DDRAM address to “00H” from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	—	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	—	—	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 μs
Function Set	0	0	0	0	1	DL	N	F	—	—	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5×11 dots/5×8 dots)	39 μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39 μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43 μs

＊ ”—”：don’t care

12-2.4 Timing characteristics

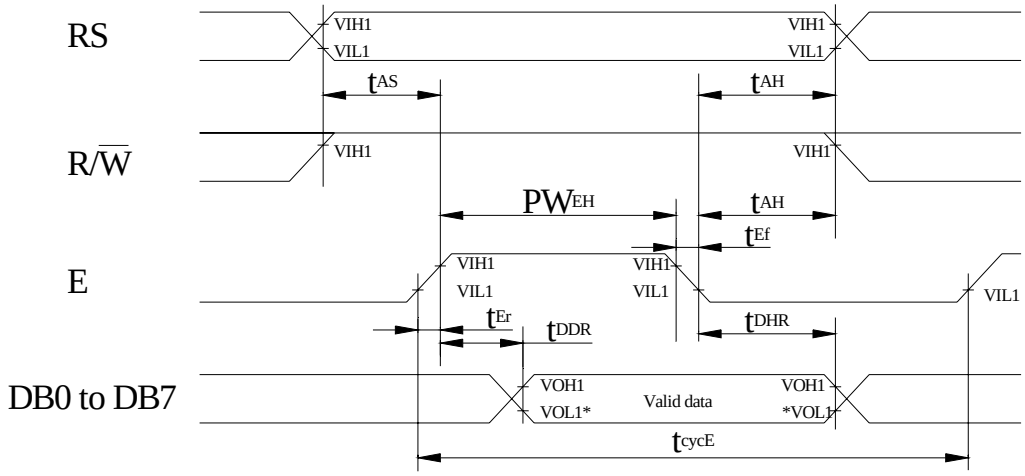
12-2.4.1Write Operation



Ta=25℃,Vdd=5.0±0.5V

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}	500	—	—	ns
Enable pulse width (high level)	PW_{EH}	230	—	—	ns
Enable rise/fall time	t_{Er},t_{Ef}	—	—	20	ns
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—	ns
Address hold time	t_{AH}	10	—	—	ns
Data set-up time	t_{DSW}	80	—	—	ns
Data hold time	t_{H}	10	—	—	ns

12-2.4.2 Read Operation



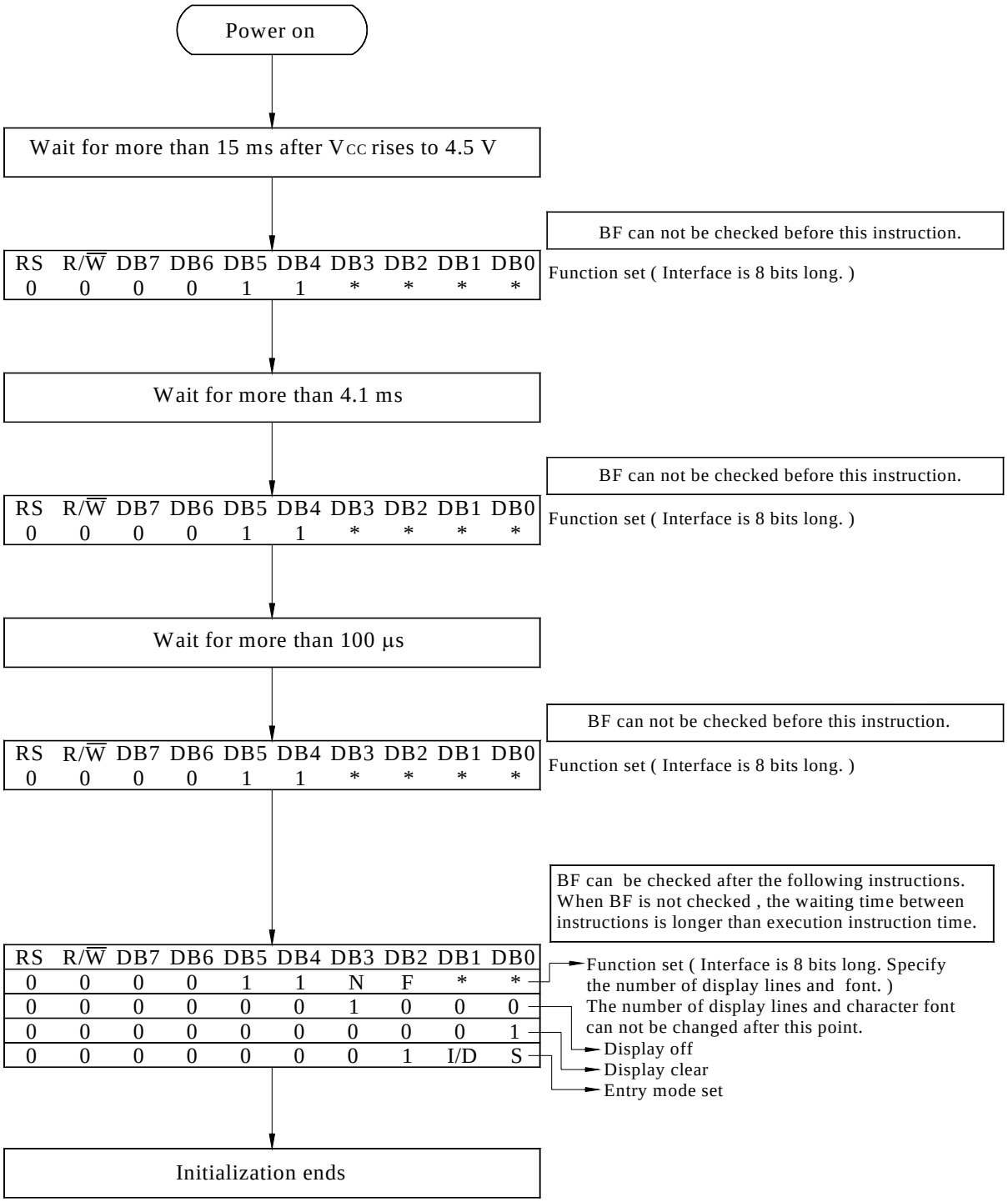
NOTE: *VOL1 is assumed to be 0.8V at 2 MHZ operation.

Ta=25℃,Vdd=5.0±0.5V

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}	500	—	—	ns
Enable pulse width (high level)	PW_{EH}	230	—	—	ns
Enable rise/fall time	t_{Er},t_{Ef}	—	—	20	ns
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—	ns
Address hold time	t_{AH}	10	—	—	ns
Data delay time	t_{DDR}	—	—	100	ns
Data hold time	t_{DHR}	5	—	—	ns

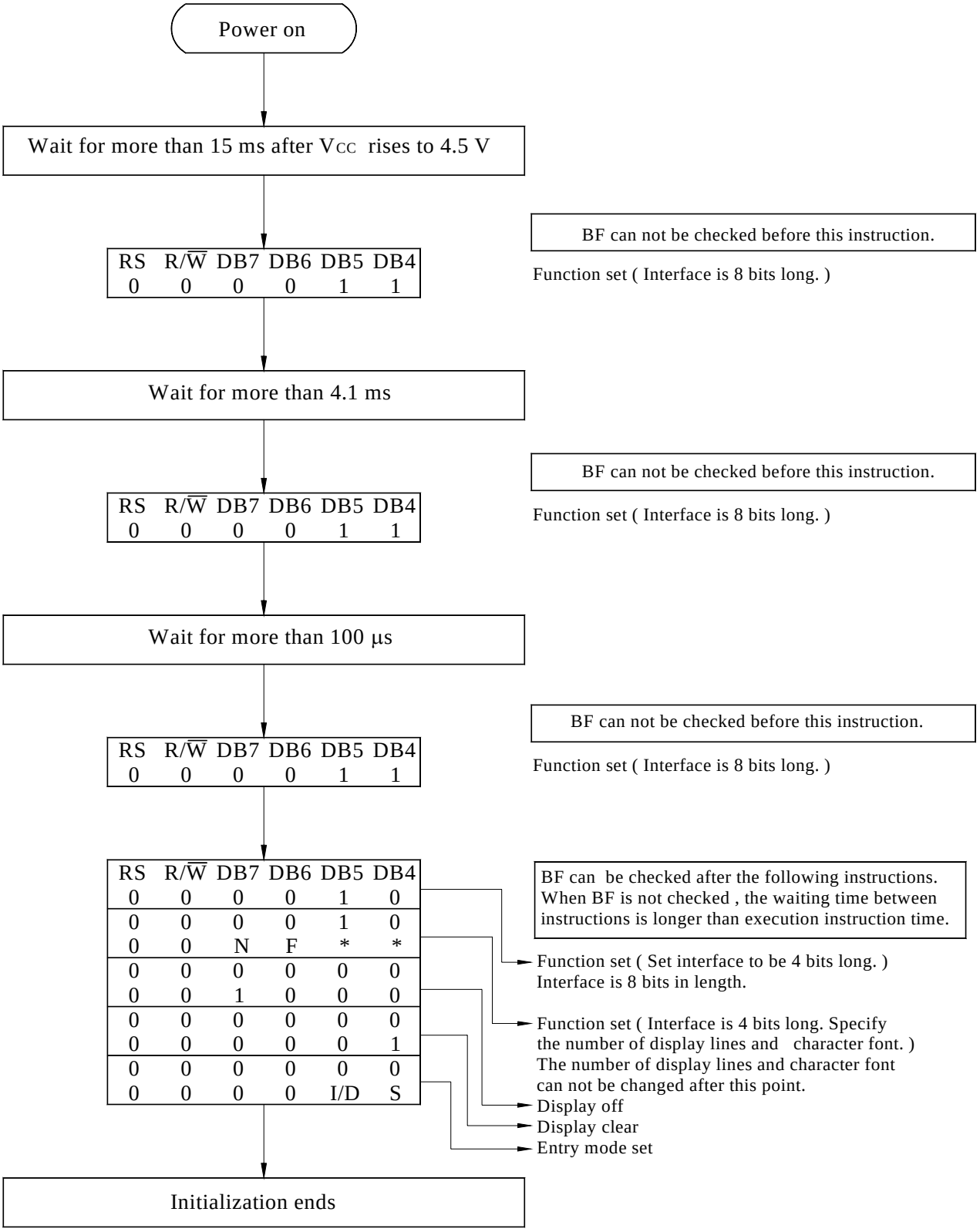
12-2.5 Initializing soft ware of LCM

12-2.5.1 8-bit interface



8-Bit Ineterface

12-2.5.2 4-bit interface



4-Bit Ineterface