

# 74HC73

## Dual JK flip-flop with reset; negative-edge trigger

Rev. 04 — 19 March 2008

Product data sheet

### 1. General description

The 74HC73 is a high-speed Si-gate CMOS device that complies with JEDEC standard no. 7A. It is pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC73 is a dual negative-edge triggered JK flip-flop featuring individual J, K, clock ( $\overline{nCP}$ ) and reset ( $\overline{nR}$ ) inputs; also complementary  $nQ$  and  $n\overline{Q}$  outputs.

The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation.

The reset ( $\overline{nR}$ ) is an asynchronous active LOW input. When LOW, it overrides the clock and data inputs, forcing the  $nQ$  output LOW and the  $n\overline{Q}$  output HIGH.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

### 2. Features

- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+80\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

### 3. Ordering information

Table 1. Ordering information

| Type number | Package                                                         |         |                                                                        |          |
|-------------|-----------------------------------------------------------------|---------|------------------------------------------------------------------------|----------|
|             | Temperature range                                               | Name    | Description                                                            | Version  |
| 74HC73N     | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | DIP14   | plastic dual in-line package; 14 leads (300 mil)                       | SOT27-1  |
| 74HC73D     | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SO14    | plastic small outline package; 14 leads; body width 3.9 mm             | SOT108-1 |
| 74HC73DB    | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | SSOP14  | plastic shrink small outline package; 14 leads; body width 5.3 mm      | SOT337-1 |
| 74HC73PW    | $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$ | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

4. Functional diagram

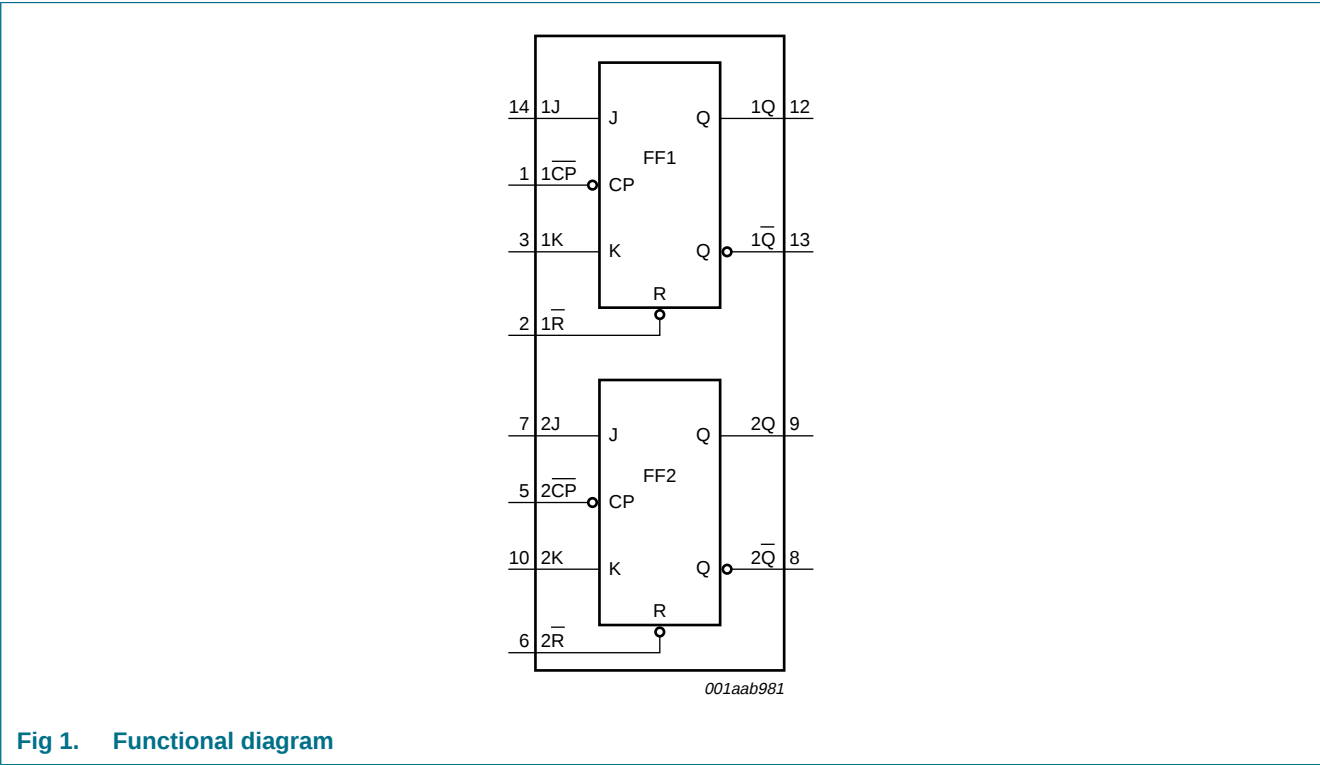


Fig 1. Functional diagram

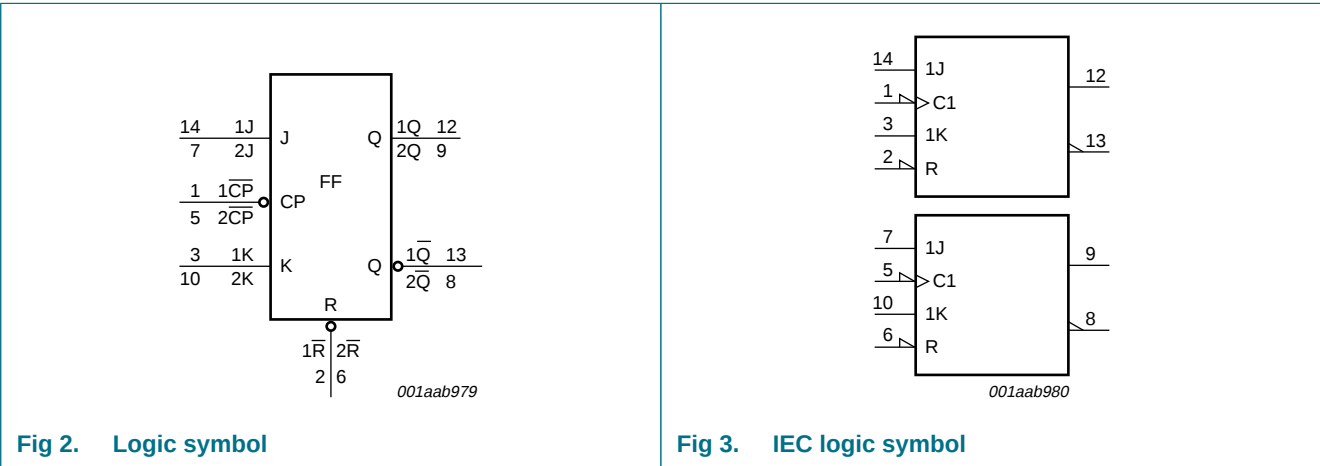
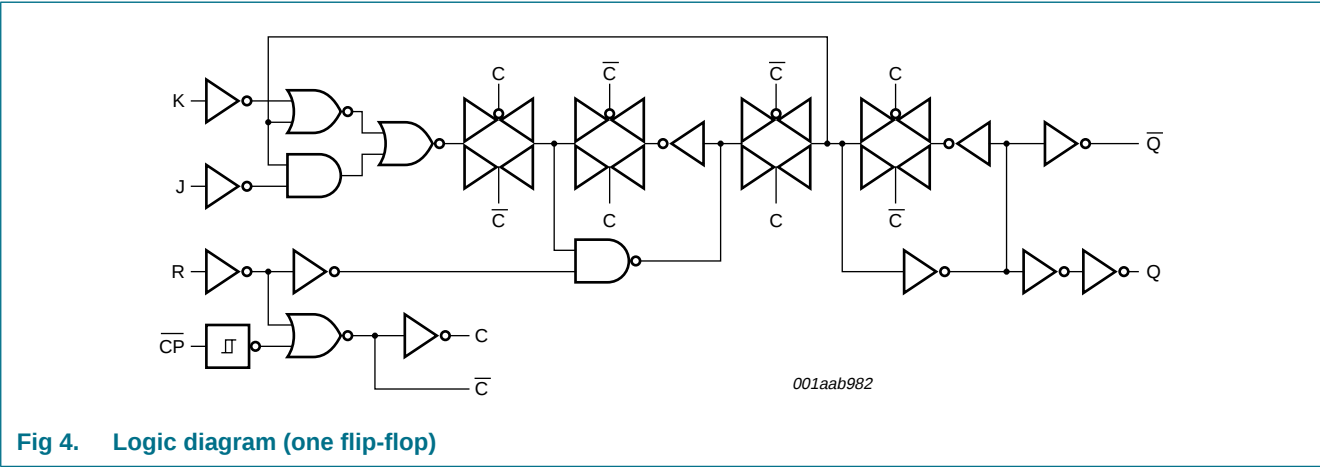


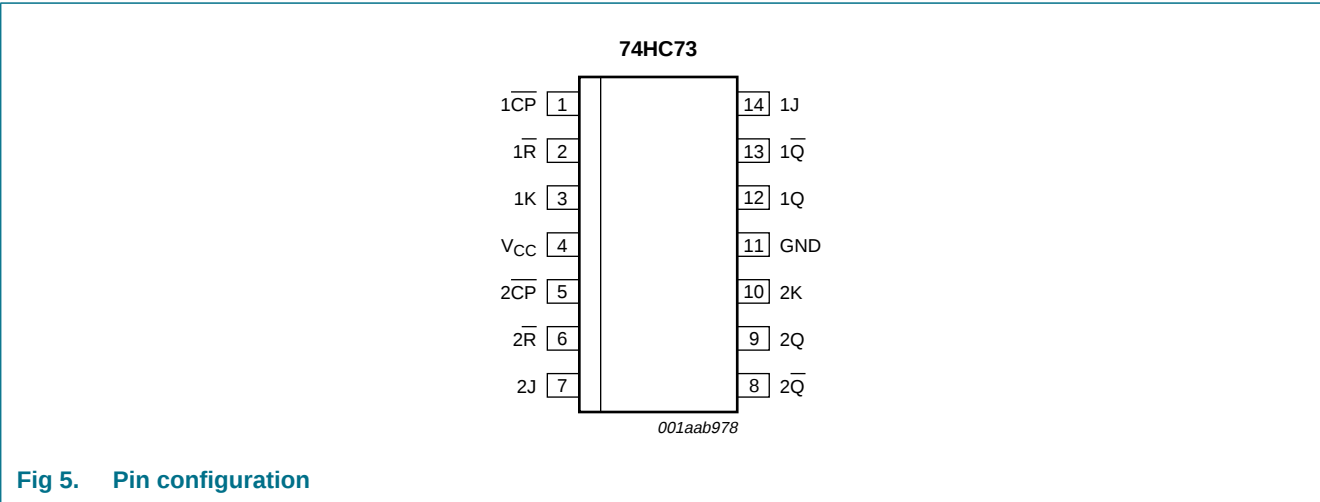
Fig 2. Logic symbol

Fig 3. IEC logic symbol



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol   | Pin   | Description                                                       |
|----------|-------|-------------------------------------------------------------------|
| 1CP, 2CP | 1, 5  | clock input (HIGH-to-LOW edge-triggered); also referred to as nCP |
| 1R, 2R   | 2, 6  | asynchronous reset input (active LOW); also referred to as nR     |
| 1K, 2K   | 3, 10 | synchronous K input; also referred to as nK                       |
| VCC      | 4     | positive supply voltage                                           |
| GND      | 11    | ground (0 V)                                                      |
| 1Q, 2Q   | 12, 9 | true output; also referred to as nQ                               |
| 1Q, 2Q   | 13, 8 | complement output; also referred to as nQ                         |
| 1J, 2J   | 14, 7 | synchronous J input; also referred to as nJ                       |

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

| Input |     |    |    | Output |    | Operating mode     |
|-------|-----|----|----|--------|----|--------------------|
| nR    | nCP | nJ | nK | nQ     | nQ |                    |
| L     | X   | X  | X  | L      | H  | asynchronous reset |
| H     | ↓   | h  | h  | q      | q  | toggle             |
| H     | ↓   | l  | h  | L      | H  | load 0 (reset)     |
| H     | ↓   | h  | l  | H      | L  | load 1 (set)       |
| H     | ↓   | l  | l  | q      | q  | hold (no change)   |

- [1] H = HIGH voltage level;  
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;  
 L = LOW voltage level;  
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;  
 q = state of referenced output one set-up time prior to the HIGH-to-LOW clock transition;  
 X = don't care;  
 ↓ = HIGH-to-LOW clock transition.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol           | Parameter               | Conditions                                                          | Min              | Max  | Unit |
|------------------|-------------------------|---------------------------------------------------------------------|------------------|------|------|
| V <sub>CC</sub>  | supply voltage          |                                                                     | -0.5             | +7.0 | V    |
| I <sub>IK</sub>  | input clamping current  | V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V | <sup>[1]</sup> - | ±20  | mA   |
| I <sub>OK</sub>  | output clamping current | V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V | <sup>[1]</sup> - | ±20  | mA   |
| I <sub>O</sub>   | output current          | V <sub>O</sub> = -0.5 V to V <sub>CC</sub> + 0.5 V                  | -                | ±25  | mA   |
| I <sub>CC</sub>  | supply current          |                                                                     | -                | 50   | mA   |
| I <sub>GND</sub> | ground current          |                                                                     | -50              | -    | mA   |
| T <sub>stg</sub> | storage temperature     |                                                                     | -65              | +150 | °C   |
| P <sub>tot</sub> | total power dissipation | T <sub>amb</sub> = -40 °C to +125 °C                                |                  |      |      |
|                  |                         | DIP14 package                                                       | <sup>[2]</sup> - | 750  | mW   |
|                  |                         | SO14 package                                                        | <sup>[3]</sup> - | 500  | mW   |
|                  |                         | (T)SSOP14 package                                                   | <sup>[4]</sup> - | 500  | mW   |

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 [2] P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.  
 [3] P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.  
 [4] P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol           | Parameter                           | Conditions              | Min | Typ  | Max             | Unit |
|------------------|-------------------------------------|-------------------------|-----|------|-----------------|------|
| V <sub>CC</sub>  | supply voltage                      |                         | 2.0 | 5.0  | 6.0             | V    |
| V <sub>I</sub>   | input voltage                       |                         | 0   | -    | V <sub>CC</sub> | V    |
| V <sub>O</sub>   | output voltage                      |                         | 0   | -    | V <sub>CC</sub> | V    |
| T <sub>amb</sub> | ambient temperature                 |                         | -40 | -    | +125            | °C   |
| Δt/ΔV            | input transition rise and fall rate | V <sub>CC</sub> = 2.0 V | -   | -    | 625             | ns   |
|                  |                                     | V <sub>CC</sub> = 4.5 V | -   | 1.67 | 139             | ns   |
|                  |                                     | V <sub>CC</sub> = 6.0 V | -   | -    | 83              | ns   |

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol          | Parameter                 | Conditions                                                                             | 25 °C |      |      | -40 °C to +85 °C |      | -40 °C to +125 °C |      | Unit |
|-----------------|---------------------------|----------------------------------------------------------------------------------------|-------|------|------|------------------|------|-------------------|------|------|
|                 |                           |                                                                                        | Min   | Typ  | Max  | Min              | Max  | Min               | Max  |      |
| V <sub>IH</sub> | HIGH-level input voltage  | V <sub>CC</sub> = 2.0 V                                                                | 1.5   | 1.2  | -    | 1.5              | -    | 1.5               | -    | V    |
|                 |                           | V <sub>CC</sub> = 4.5 V                                                                | 3.15  | 2.4  | -    | 3.15             | -    | 3.15              | -    | V    |
|                 |                           | V <sub>CC</sub> = 6.0 V                                                                | 4.2   | 3.2  | -    | 4.2              | -    | 4.2               | -    | V    |
| V <sub>IL</sub> | LOW-level input voltage   | V <sub>CC</sub> = 2.0 V                                                                | -     | 0.8  | 0.5  | -                | 0.5  | -                 | 0.5  | V    |
|                 |                           | V <sub>CC</sub> = 4.5 V                                                                | -     | 2.1  | 1.35 | -                | 1.35 | -                 | 1.35 | V    |
|                 |                           | V <sub>CC</sub> = 6.0 V                                                                | -     | 2.8  | 1.8  | -                | 1.8  | -                 | 1.8  | V    |
| V <sub>OH</sub> | HIGH-level output voltage | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                    |       |      |      |                  |      |                   |      |      |
|                 |                           | I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V                                       | 1.9   | 2.0  | -    | 1.9              | -    | 1.9               | -    | V    |
|                 |                           | I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V                                       | 4.4   | 4.5  | -    | 4.4              | -    | 4.4               | -    | V    |
|                 |                           | I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V                                       | 5.9   | 6.0  | -    | 5.9              | -    | 5.9               | -    | V    |
|                 |                           | I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 4.5 V                                        | 3.98  | 4.32 | -    | 3.84             | -    | 3.7               | -    | V    |
| V <sub>OL</sub> | LOW-level output voltage  | I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V                                      | 5.48  | 5.81 | -    | 5.34             | -    | 5.2               | -    | V    |
|                 |                           | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                    |       |      |      |                  |      |                   |      |      |
|                 |                           | I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V                                        | -     | 0    | 0.1  | -                | 0.1  | -                 | 0.1  | V    |
|                 |                           | I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V                                        | -     | 0    | 0.1  | -                | 0.1  | -                 | 0.1  | V    |
|                 |                           | I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V                                        | -     | 0    | 0.1  | -                | 0.1  | -                 | 0.1  | V    |
| I <sub>I</sub>  | input leakage current     | I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 4.5 V                                         | -     | 0.15 | 0.26 | -                | 0.33 | -                 | 0.4  | V    |
|                 |                           | I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V                                       | -     | 0.16 | 0.26 | -                | 0.33 | -                 | 0.4  | V    |
|                 |                           | V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V                       | -     | -    | ±0.1 | -                | ±1.0 | -                 | ±1.0 | μA   |
| I <sub>CC</sub> | supply current            | V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V | -     | -    | 4.0  | -                | 40.0 | -                 | 80.0 | μA   |
| C <sub>I</sub>  | input capacitance         |                                                                                        | -     | 3.5  | -    | -                | -    | -                 | -    | pF   |

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 8](#)

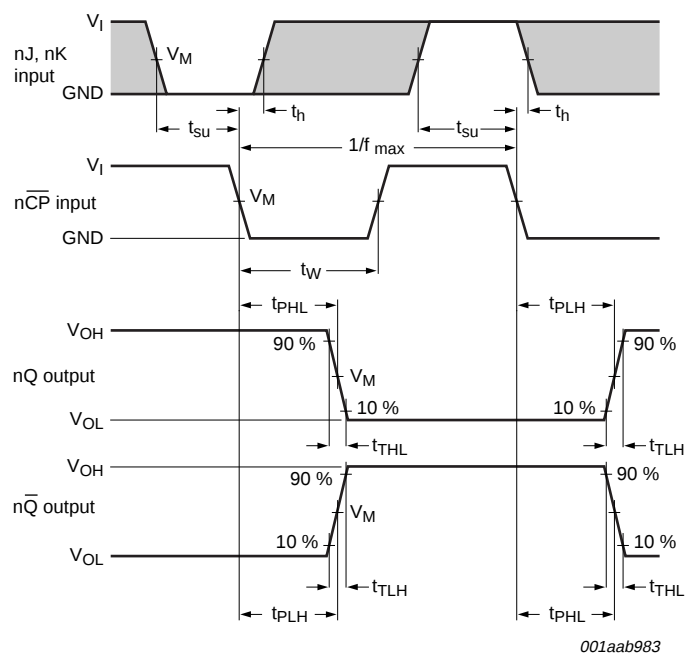
| Symbol    | Parameter         | Conditions                                                            | 25 °C |     |     | –40 °C to +85 °C |     | –40 °C to +125 °C |     | Unit |
|-----------|-------------------|-----------------------------------------------------------------------|-------|-----|-----|------------------|-----|-------------------|-----|------|
|           |                   |                                                                       | Min   | Typ | Max | Min              | Max | Min               | Max |      |
| $t_{pd}$  | propagation delay | $\overline{nCP}$ to nQ; see <a href="#">Figure 6</a> <sup>[1]</sup>   |       |     |     |                  |     |                   |     |      |
|           |                   | $V_{CC} = 2.0$ V                                                      | -     | 52  | 160 | -                | 200 | -                 | 240 | ns   |
|           |                   | $V_{CC} = 4.5$ V                                                      | -     | 19  | 32  | -                | 40  | -                 | 48  | ns   |
|           |                   | $V_{CC} = 6.0$ V                                                      | -     | 15  | 27  | -                | 34  | -                 | 41  | ns   |
|           |                   | $V_{CC} = 5.0$ V; $C_L = 15$ pF                                       | -     | 16  | -   | -                | -   | -                 | -   | ns   |
|           |                   | $\overline{nCP}$ to $\overline{nQ}$ ; see <a href="#">Figure 6</a>    |       |     |     |                  |     |                   |     |      |
|           |                   | $V_{CC} = 2.0$ V                                                      | -     | 52  | 160 | -                | 200 | -                 | 240 | ns   |
|           |                   | $V_{CC} = 4.5$ V                                                      | -     | 19  | 32  | -                | 40  | -                 | 48  | ns   |
|           |                   | $V_{CC} = 6.0$ V                                                      | -     | 15  | 27  |                  | 34  | -                 | 41  | ns   |
|           |                   | $V_{CC} = 5.0$ V; $C_L = 15$ pF                                       | -     | 16  | -   | -                | -   |                   |     | ns   |
|           |                   | $\overline{nR}$ to nQ, $\overline{nQ}$ ; see <a href="#">Figure 7</a> |       |     |     |                  |     |                   |     |      |
|           |                   | $V_{CC} = 2.0$ V                                                      | -     | 50  | 145 | -                | 180 | -                 | 220 | ns   |
|           |                   | $V_{CC} = 4.5$ V                                                      | -     | 18  | 29  | -                | 36  | -                 | 44  | ns   |
|           |                   | $V_{CC} = 6.0$ V                                                      | -     | 14  | 25  |                  | 31  | -                 | 38  | ns   |
|           |                   | $V_{CC} = 5.0$ V; $C_L = 15$ pF                                       | -     | 15  | -   | -                | -   | -                 | -   | ns   |
| $t_t$     | transition time   | nQ, $\overline{nQ}$ ; see <a href="#">Figure 6</a> <sup>[2]</sup>     |       |     |     |                  |     |                   |     |      |
|           |                   | $V_{CC} = 2.0$ V                                                      | -     | 19  | 75  | -                | 95  | -                 | 110 | ns   |
|           |                   | $V_{CC} = 4.5$ V                                                      | -     | 7   | 15  | -                | 19  | -                 | 22  | ns   |
|           |                   | $V_{CC} = 6.0$ V                                                      | -     | 6   | 13  |                  | 16  | -                 | 19  | ns   |
| $t_w$     | pulse width       | $\overline{nCP}$ input, HIGH or LOW; see <a href="#">Figure 6</a>     |       |     |     |                  |     |                   |     |      |
|           |                   | $V_{CC} = 2.0$ V                                                      | 80    | 22  | -   | 100              |     | 120               | -   | ns   |
|           |                   | $V_{CC} = 4.5$ V                                                      | 16    | 8   | -   | 20               | -   | 24                | -   | ns   |
|           |                   | $V_{CC} = 6.0$ V                                                      | 14    | 6   | -   | 17               | -   | 20                |     | ns   |
|           |                   | $\overline{nR}$ input, HIGH or LOW; see <a href="#">Figure 7</a>      |       |     |     |                  |     |                   |     |      |
|           |                   | $V_{CC} = 2.0$ V                                                      | 80    | 22  | -   | 100              |     | 120               | -   | ns   |
|           |                   | $V_{CC} = 4.5$ V                                                      | 16    | 8   | -   | 20               | -   | 24                | -   | ns   |
|           |                   | $V_{CC} = 6.0$ V                                                      | 14    | 6   | -   | 17               | -   | 20                |     | ns   |
| $t_{rec}$ | recovery time     | $\overline{nR}$ to $\overline{nCP}$ ; see <a href="#">Figure 7</a>    |       |     |     |                  |     |                   |     |      |
|           |                   | $V_{CC} = 2.0$ V                                                      | 80    | 22  | -   | 100              |     | 120               | -   | ns   |
|           |                   | $V_{CC} = 4.5$ V                                                      | 16    | 8   | -   | 20               | -   | 24                | -   | ns   |
|           |                   | $V_{CC} = 6.0$ V                                                      | 14    | 6   | -   | 17               | -   | 20                |     | ns   |
| $t_{su}$  | set-up time       | nJ, nK to $\overline{nCP}$ ; see <a href="#">Figure 6</a>             |       |     |     |                  |     |                   |     |      |
|           |                   | $V_{CC} = 2.0$ V                                                      | 80    | 22  | -   | 100              |     | 120               | -   | ns   |
|           |                   | $V_{CC} = 4.5$ V                                                      | 16    | 8   | -   | 20               | -   | 24                | -   | ns   |
|           |                   | $V_{CC} = 6.0$ V                                                      | 14    | 6   | -   | 17               | -   | 20                |     | ns   |

**Table 7. Dynamic characteristics ...continued**GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 8](#)

| Symbol    | Parameter                     | Conditions                                                | 25 °C |     |     | –40 °C to +85 °C |     | –40 °C to +125 °C |     | Unit |
|-----------|-------------------------------|-----------------------------------------------------------|-------|-----|-----|------------------|-----|-------------------|-----|------|
|           |                               |                                                           | Min   | Typ | Max | Min              | Max | Min               | Max |      |
| $t_h$     | hold time                     | nJ, nK to $\overline{nCP}$ ; see <a href="#">Figure 6</a> |       |     |     |                  |     |                   |     |      |
|           |                               | $V_{CC} = 2.0$ V                                          | 3     | –8  | –   | 3                |     | 3                 | –   | ns   |
|           |                               | $V_{CC} = 4.5$ V                                          | 3     | –3  | –   | 3                | –   | 3                 | –   | ns   |
|           |                               | $V_{CC} = 6.0$ V                                          | 3     | –2  | –   | 3                | –   | 3                 |     | ns   |
| $f_{max}$ | maximum frequency             | $\overline{nCP}$ input; see <a href="#">Figure 6</a>      |       |     |     |                  |     |                   |     |      |
|           |                               | $V_{CC} = 2.0$ V                                          | 6.0   | 23  | –   | 4.8              |     | 4.0               | –   | MHz  |
|           |                               | $V_{CC} = 4.5$ V                                          | 30    | 70  | –   | 24               | –   | 20                | –   | MHz  |
|           |                               | $V_{CC} = 6.0$ V                                          | 35    | 83  | –   | 28               | –   | 24                | –   | MHz  |
| $C_{PD}$  | power dissipation capacitance | per flip-flop; $V_I = \text{GND to } V_{CC}$              | [3]   | –   | 30  | –                | –   | –                 | –   | pF   |

[1]  $t_{pd}$  is the same as  $t_{PHL}$ ,  $t_{PLH}$ .[2]  $t_t$  is the same as  $t_{THL}$ ,  $t_{TLH}$ .[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where: $f_i$  = input frequency in MHz; $f_o$  = output frequency in MHz; $C_L$  = output load capacitance in pF; $V_{CC}$  = supply voltage in V; $N$  = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## 11. Waveforms

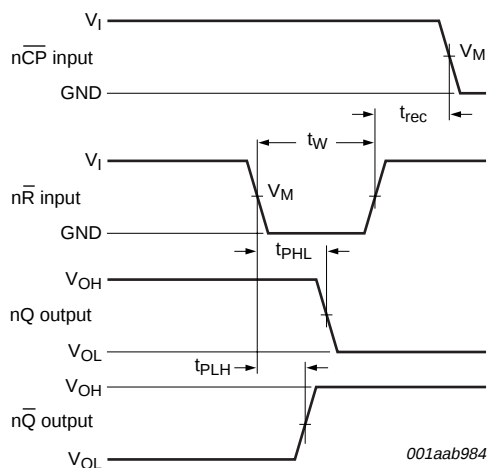


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 6. Waveforms showing the clock ( $\overline{nCP}$ ) to output ( $nQ$ ,  $\overline{nQ}$ ) propagation delays, the clock pulse width, the J and K to  $\overline{nCP}$  set and hold times, the output transition times and the maximum clock frequency**



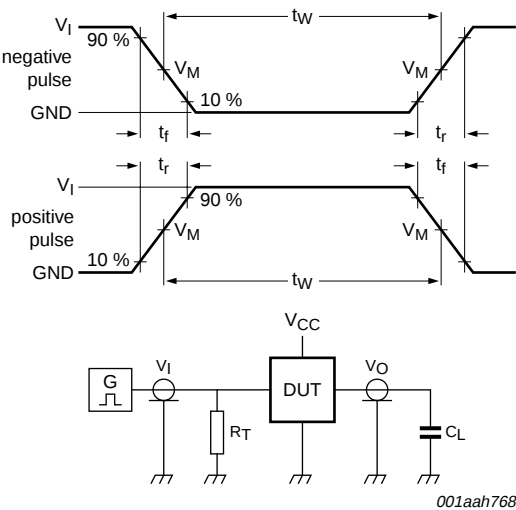
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig 7. Waveforms showing the reset ( $\overline{nR}$ ) input to output ( $nQ$ ,  $\overline{nQ}$ ) propagation delays and the reset pulse width and the  $\overline{nR}$  to  $\overline{nCP}$  removal time**

Table 8. Measurement points

| Type   | Input    |             | Output      |
|--------|----------|-------------|-------------|
|        | $V_I$    | $V_M$       | $V_M$       |
| 74HC73 | $V_{CC}$ | $0.5V_{CC}$ | $0.5V_{CC}$ |



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

| Type   | Input    |            | Load         |
|--------|----------|------------|--------------|
|        | $V_I$    | $t_r, t_f$ | $C_L$        |
| 74HC73 | $V_{CC}$ | 6 ns       | 15 pF, 50 pF |

12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

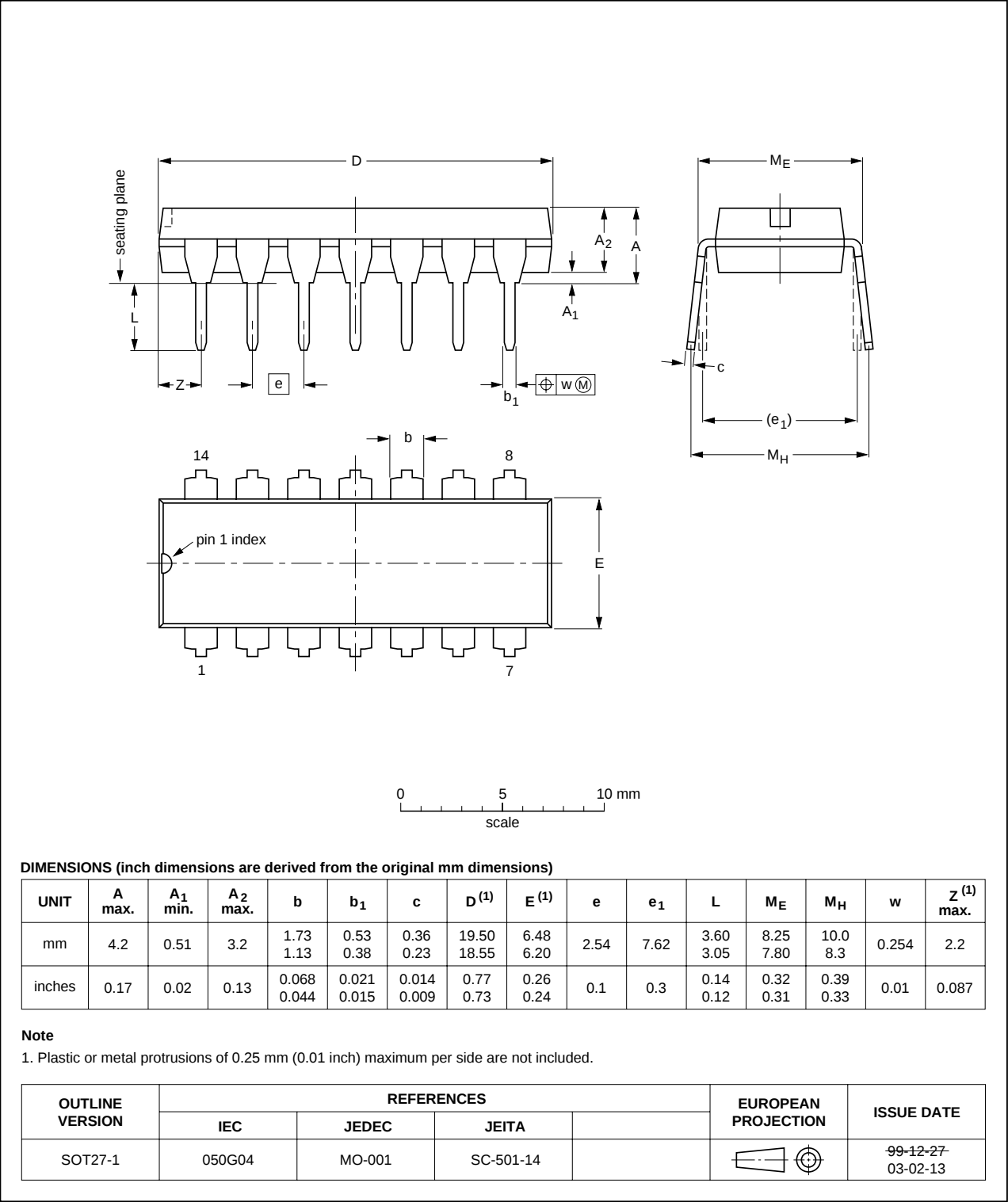


Fig 9. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

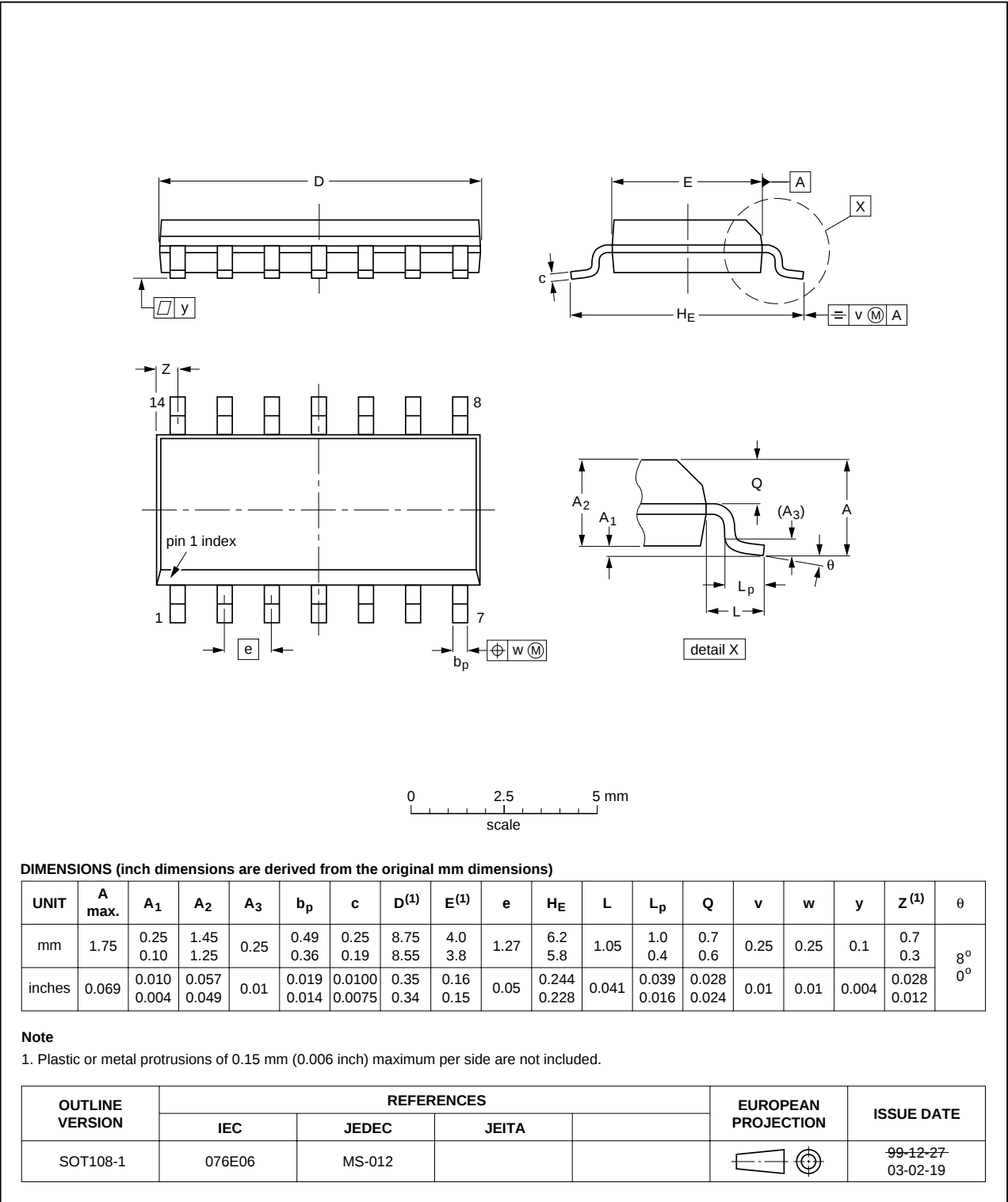


Fig 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

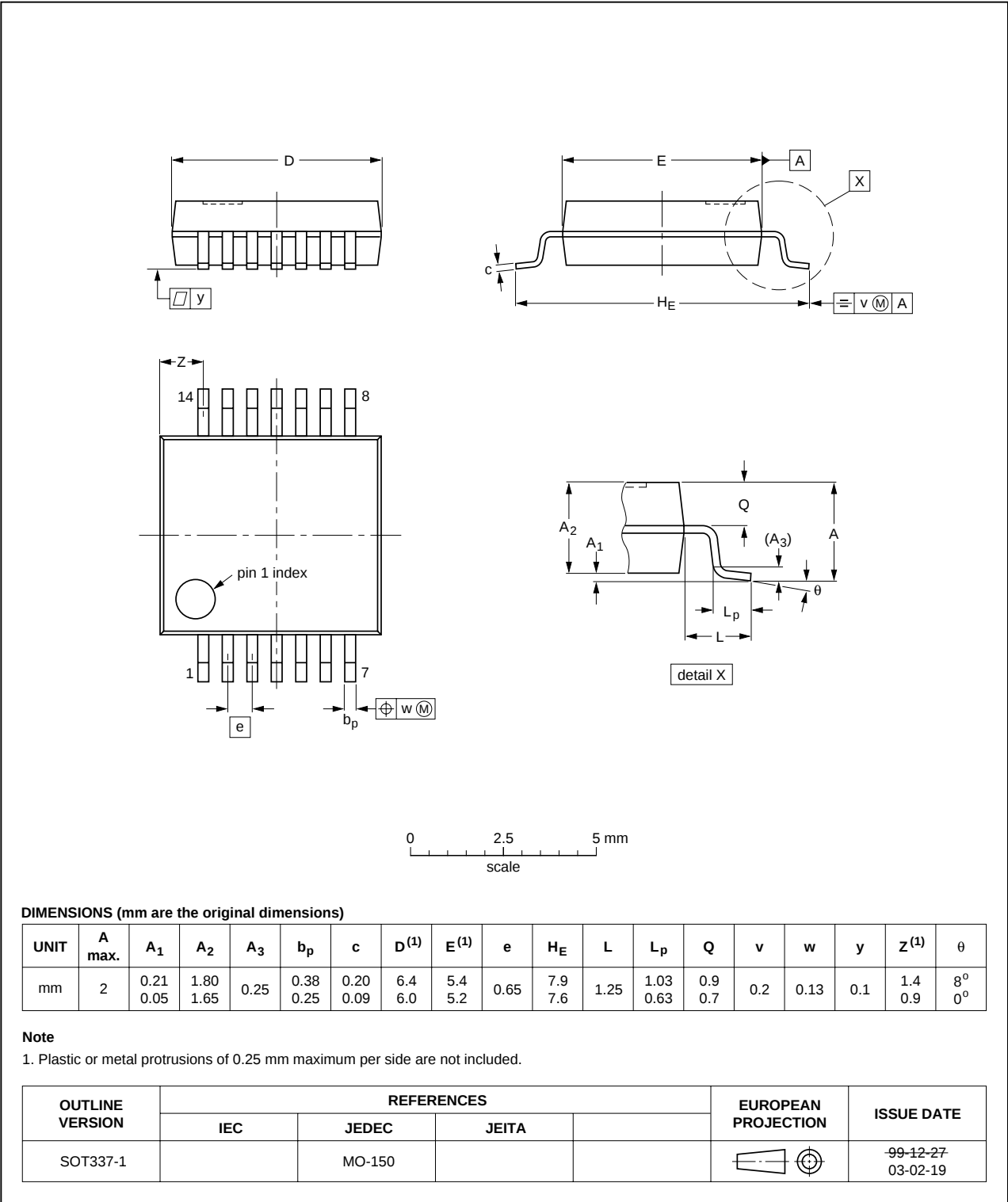


Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

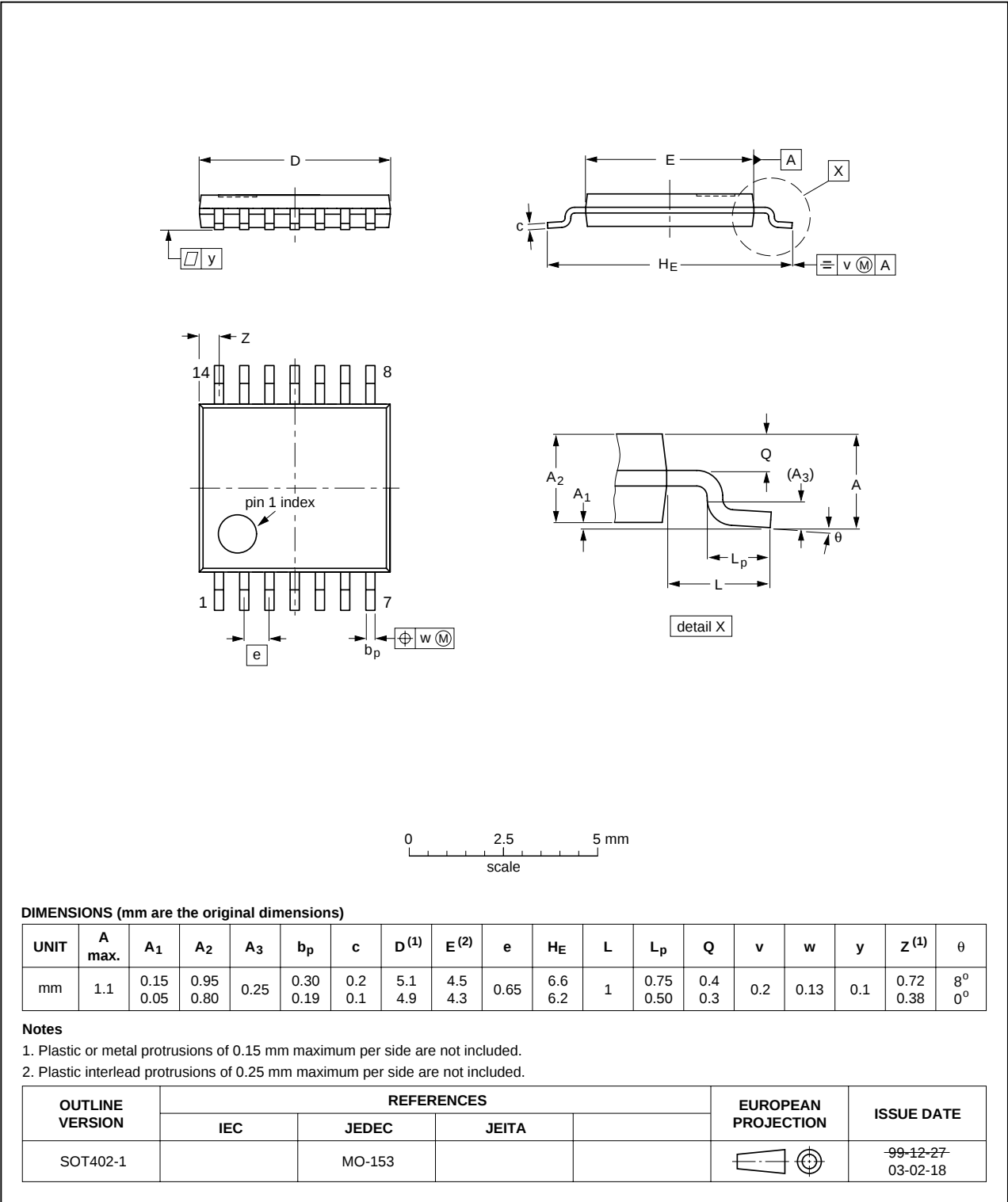


Fig 12. Package outline SOT402-1 (TSSOP14)

## 13. Abbreviations

Table 10. Abbreviations

| Acronym | Description                             |
|---------|-----------------------------------------|
| CMOS    | Complementary Metal-Oxide Semiconductor |
| DUT     | Device Under Test                       |
| ESD     | ElectroStatic Discharge                 |
| HBM     | Human Body Model                        |
| MM      | Machine Model                           |
| TTL     | Transistor-Transistor Logic             |

## 14. Revision history

Table 11. Revision history

| Document ID      | Release date                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Data sheet status     | Change notice | Supersedes       |
|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|---------------|------------------|
| 74HC73_4         | 20080319                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Product data sheet    | -             | 74HC73_3         |
| Modifications:   | <ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Quick reference data incorporated into <a href="#">Section 9</a> and <a href="#">10</a>.</li><li>• <a href="#">Section 8 "Recommended operating conditions"</a> <math>t_r</math>, <math>t_f</math> converted to <math>\Delta t/\Delta V</math>.</li></ul> |                       |               |                  |
| 74HC73_3         | 20041112                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Product data sheet    | -             | 74HC_HCT73_CNV_2 |
| 74HC_HCT73_CNV_2 | December 1990                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Product specification | -             | -                |

## 15. Legal information

### 15.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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